

BANDON/NorthBay 13" Schematics Document

Whiskey Lake -U 42

2019-02-12

REV:A00

DY : None Installed
WWAN:For WWAN installed
LAN:For LAN Installed
Sensor:For Sensor Installed
Debug:For Debug Port installed

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Bandon / NorthBay 13"

Rev
X00

Date: Friday, February 15, 2019

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Project code : 4PD0G3010001
PCB P/N : 18717
Revision : -1

Lat Function	R45/Transformer	Bandon	NorthBay
Lat Function	Lat IC	De-pop	Pop
Sensor Board	E-compass	Pop	De-pop
	Accelerometer + Gyro	Pop	De-pop
	P-sensor	Pop	De-pop
Lat Board	Led	Pop	Pop
	Hall sensor	Pop	De-pop

eDP 13" Panel
55

Touch Panel
55

Intel CPU
WHISKEY LAKE-U 42
WHL U PCH-LP
16 PCIe* Lanes
3 SATA Lanes
6 USB3.1 Gen1/Gen2 Lanes
5 GbE Lanes
2 Remapped PCIe* storage

DDR4 Channel A
DDR4 2400
SODIMM A 12

DDR4 Channel B
DDR4 2400
SODIMM B 13

Bandon/Northbay 13" Block Diagram

NON-INTERLEAVE MODE

USB PowerShare
SILEGO
SLGC55544CVTR 36

USB3.1 / PowerShare
USB Port : 2
35

USB2.0 [3]
USB3.1 [3] GEN1

USB2.0 [2]
USB3.1 [2] GEN1

USB3.1
USB Port : 1
35

Internal Digital MIC
Camera 55

Universal Jack
(2W, 4ohm /channel)
2CH Speaker

Audio Codec
RealTek
ALC3254 27

Flash ROM
WSON
Winbond
W25Q64JVEIQ (8MB) non-Vpro SRU
W25Q256JVEIQ (32MB) Vpro SRU

Flash ROM
SOP8
Winbond
W25Q128JVEIQ (16MB) non-Vpro

TPM 2.0
ST
ST33TPHF2XSPI
[Co-lay Nuvoton 750] 91

EC
SMSC
MEC 5106 24

KB/TP Conn
65

Thermal & Fan
26

eSPI debug port
68

Hall sensor
BANDON NORTHBAY
TCS40DLR APX8131A 67

LED BD
64

Finger Printer
92

CV3 Lynx Controller
Broadcom
BCM58202 66

FLASH ROM
SOP8 6*5
Winbond
MX25L12872FM2I (16MB)

RFID/NFC
RFID Antenna

SmartCard IC
NXP
TDA8034HN

Connector
Smart Card

Accelerometer
ST
LNG2DMTR 70

E-compass
ST
LIS2MDLTR

Accelerometer + Gyro
ST
LSM6DSUSTR


P-sensor
SEMTECH
SX9310

I2C

Sensor BD
De-pop on NorthBay

Charger ISL9538HRTZ-GP-U 44	
INPUTS	OUTPUTS
BT+	DCBATOUT
SYSTEM DC/DC SY8288BRAC/SY8288CRAC 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_AUX_S5 5V_S5
CPU DC/DC FDMF3035-GP 47	
INPUTS	OUTPUTS
DCBATOUT	1V_VCCGT
CPU DC/DC ISL95808HRZ-T-1-GP 50	
INPUTS	OUTPUTS
DCBATOUT	1V_VCCSA
SYSTEM DC/DC SY8288RAC 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3
SYSTEM DC/DC AOZ2260QI-10-GP 52	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5
SYSTEM DC/DC RT6542AGQW-GP 54	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VCCPRIM_CORE
Load Switches	
INPUTS	OUTPUTS
3D3V_S5	3D3V_S5_PCH 3D3V_LAN 3D3V_S5_WWAN 3D3V_S5_WLAN 2D5V_S3 1D8V_S5 VCDVDD_FUSE 3D3V_S0
3D3V_S0	+3V_AVDD 3D3V_CAMERA_S0 3D3V_S0_SATA
5V_S5	5V_S0 1D05V_VCCIO
5V_S0	+5V_PVDD 5V_TSP_S0 5V_HDMI
1D8V_S5	1D8V_S0
1D2V_S3	0D6V_S0 1D2V_VCCPLL_OC
1D05V_S5	1D05V_VCCSTG 1D05V_VCCSTG
PCB LAYER (FR4-10 Layer)	
L1: Top L2: GND L3: Signal L4: GND L5: Signal	L6: Signal L7: GND/PWR L8: Signal L9: GND L10: Bottom

<Core Design>



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Block Diagram

Bandon / NorthBay 13"

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Size:
Date: Friday, February 18, 2016

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Main Func = CPU

[24]	PECI_CPU	<< >>
[24,43,44,46]	PROCHOT#_CPU	<< >>
[24]	THERMTRIP#_CPU	<< >>
[99]	BPM_N0	<<< >>>
[99]	BPM_N1	<<< >>>
[99]	CPU_JTAG_TCK	<< >>
[99]	CPU_JTAG_TDI	<< >>
[99]	CPU_JTAG_TDO	<< >>
[99]	CPU_JTAG_TMS	<< >>
[99]	CPU_JTAG_TRST#	<< >>
[99]	CPU_JTAG_PRDY#	<< >>
[99]	CPU_JTAG_PREQ#	<< >>
[99]	PCH_JTAG_TCK	<< >>
[17]	H_CUPWRGD	>> >>
[55]	TOUCH_SCREEN_PD#_R	>> >>
[24,65]	TOUCHPAD_INTR#	>> >>
[55]	TOUCH_SCREEN_DET#	>> >>

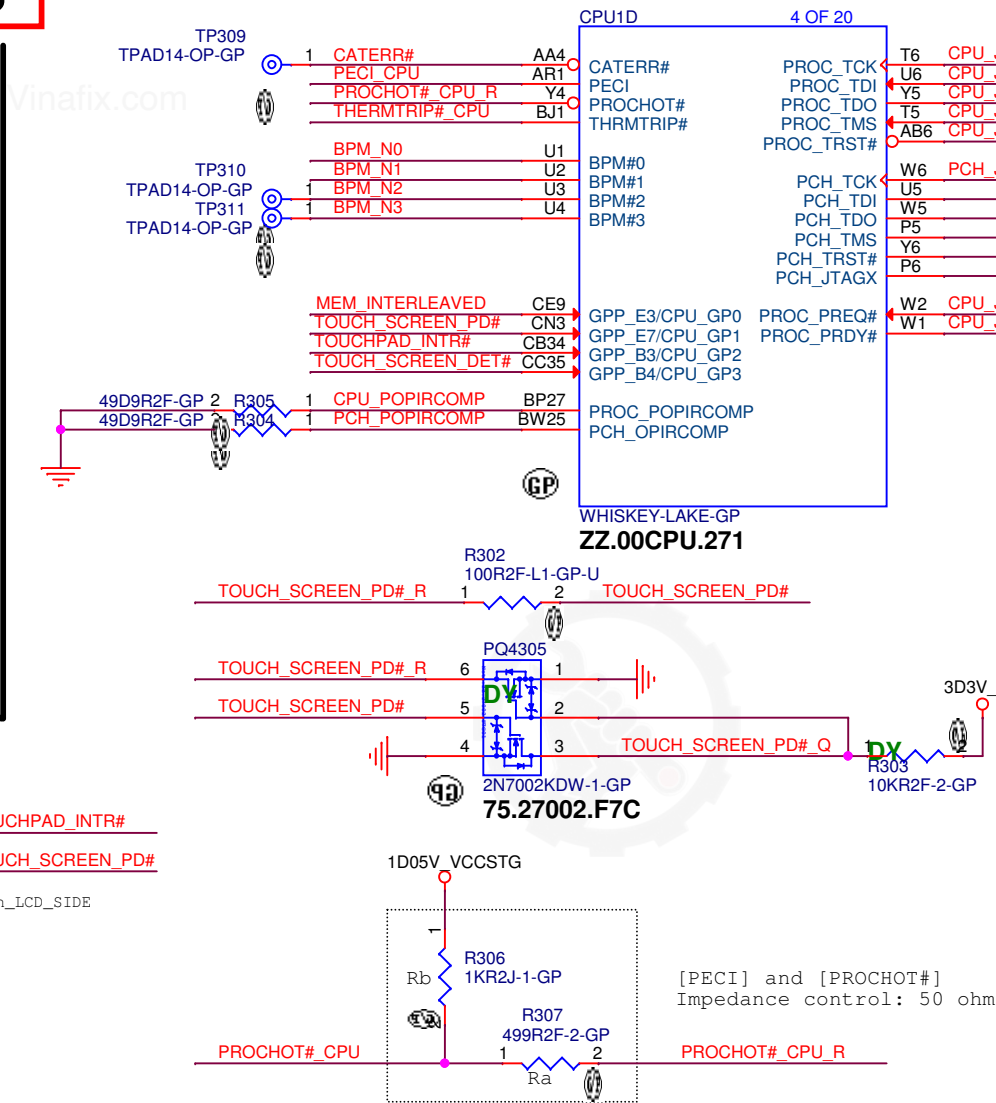
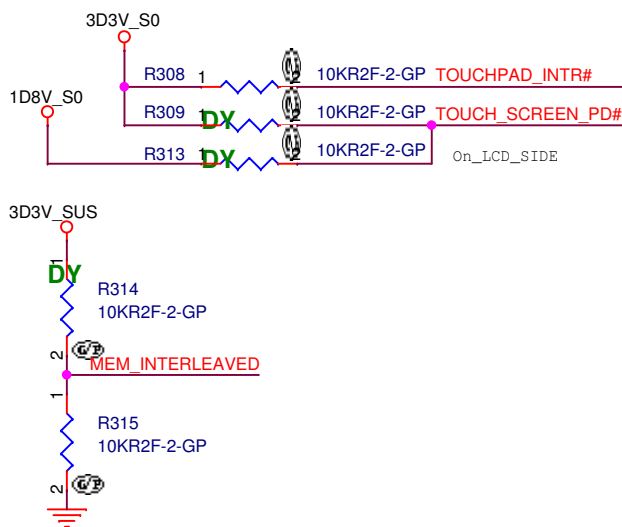
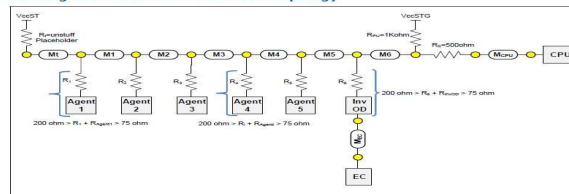


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

<Core Design>



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Title (Reserved)		
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Main Func = CPU

Edp

[55] eDP_TX_CPU_N0 <<<
[55] eDP_TX_CPU_P0 <<<
[55] eDP_TX_CPU_N1 <<<
[55] eDP_TX_CPU_P1 <<<

[55] eDP_AUX_CPU_N <<<
[55] eDP_AUX_CPU_P <<<

[55] EDP_HPD >>>

[55] eDP_BLEN_CPU <<<
[55] eDP_BLCTRL_CPU <<<
[55] eDP_VDDEN_CPU <<<

DP to AR

[71] DP_DDI_TX_N0 <<<
[71] DP_DDI_TX_P0 <<<
[71] DP_DDI_TX_N1 <<<
[71] DP_DDI_TX_P1 <<<
[71] DP_DDI_TX_N2 <<<
[71] DP_DDI_TX_P2 <<<
[71] DP_DDI_TX_N3 <<<
[71] DP_DDI_TX_P3 <<<

[71] DP_AUX_CPU_N <<<
[71] DP_AUX_CPU_P <<<

[71] DP_HPD_CPU >>>

[71] CPU_DP_CTRL_DATA <<<
[71] CPU_DP_CTRL_CLK <<<

DP to AR

[71] DP2_DDI_TX_N0 <<<
[71] DP2_DDI_TX_P0 <<<
[71] DP2_DDI_TX_N1 <<<
[71] DP2_DDI_TX_P1 <<<
[71] DP2_DDI_TX_N2 <<<
[71] DP2_DDI_TX_P2 <<<
[71] DP2_DDI_TX_N3 <<<
[71] DP2_DDI_TX_P3 <<<

[71] DP2_AUX_CPU_P <<<
[71] DP2_AUX_CPU_N <<<

[71] DP2_HPD_CPU <<<

DP to AR

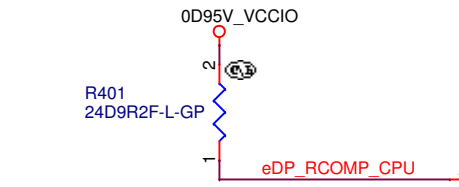
Vinafix.com

DP to AR

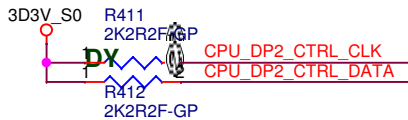
575412
eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω \pm 1%	600 mils

Note: Must maintain low DC resistance routing (<0.1 Ω)



PH/PL on TBT Page



		CPU (TBT, DP1.4, USB3.1 g2)				
Canon Lake U PCH-LP		eDP DDI A	DDI 1	DDI 2		
North Bay 13 Bandon	13 UU (non-TBT)	LCD	HDMI 1.4	Type-C Port 1		
	13 UU (TBT)	LCD	TBT (Alpine Ridge Port 0)	TBT (Alpine Ridge Port 1)	HDMI on AR side-port	

CPU1A

DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

1 OF 20

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUX_N
EDP_AUX_P
DISP_UTILS
DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUX_N
EDP_AUX_P
DISP_UTILS
DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUX_N
EDP_AUX_P
DISP_UTILS
DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUX_N
EDP_AUX_P
DISP_UTILS
DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

For AR

CN6 DP_HPD_CPU_R
CM6 DP2_HPD_CPU_R
CP7
CP6 FFS_INT2
CM7 EDP_HPD

CK11 eDP_BLEN_CPU
CG11 eDP_VDDEN_CPU
CH11 eDP_BLCTRL_CPU

3D3V_S5_PCH
R405 10KR2J-3-GP

3D3V_S5_PCH
R406 10KR2J-3-GP

3D3V_S5_PCH
R407 10KR2J-3-GP

3D3V_S5_PCH
R408 10KR2J-3-GP

3D3V_S5_PCH
R409 10KR2J-3-GP

3D3V_S5_PCH
R410 10KR2J-3-GP

3D3V_S5_PCH
R411 10KR2J-3-GP

3D3V_S5_PCH
R412 10KR2J-3-GP

3D3V_S5_PCH
R413 10KR2J-3-GP

3D3V_S5_PCH
R414 10KR2J-3-GP

3D3V_S5_PCH
R415 10KR2J-3-GP

3D3V_S5_PCH
R416 10KR2J-3-GP

3D3V_S5_PCH
R417 10KR2J-3-GP

<Core Design>



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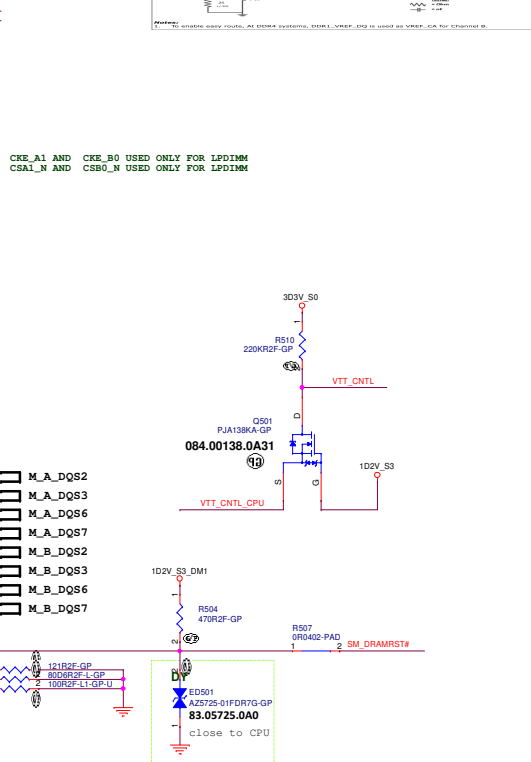
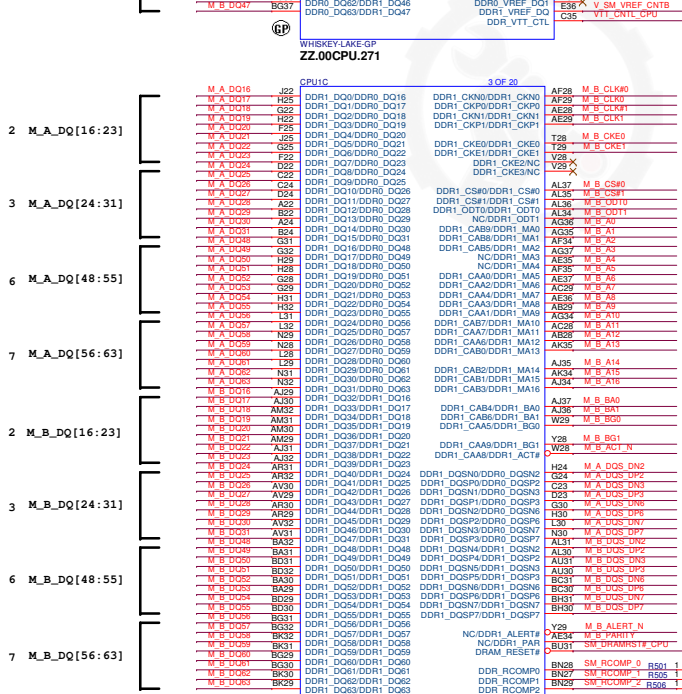
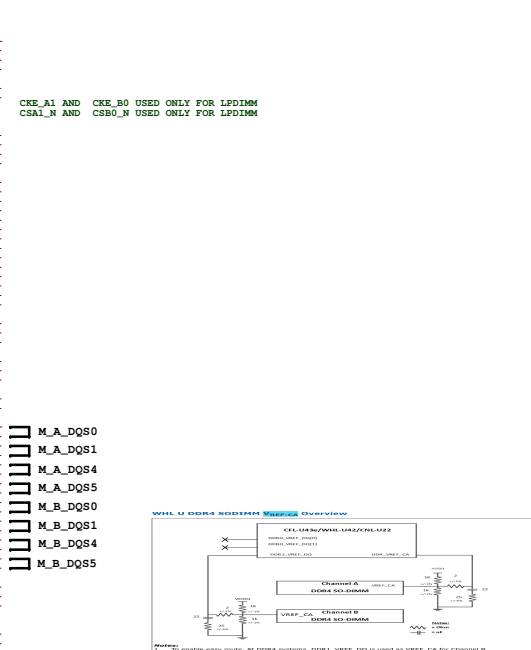
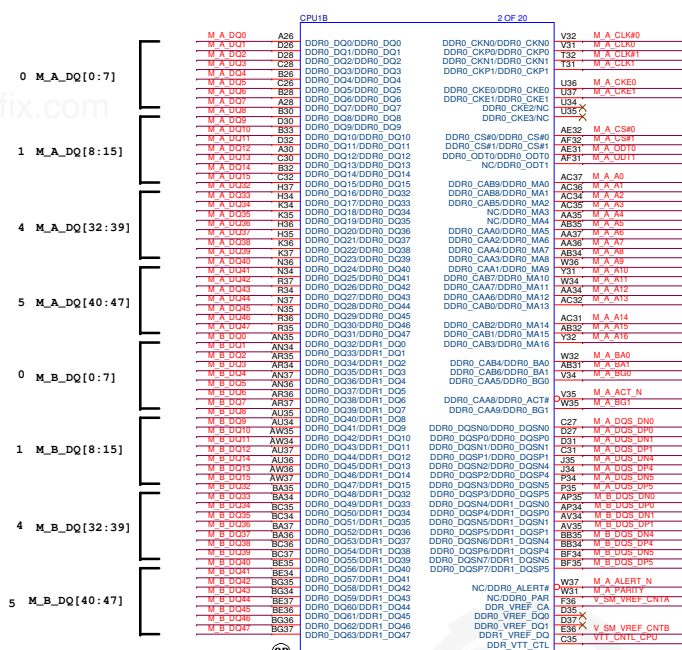
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Title CPU_(JTAG/CPU SIDE BAND)


Size A4 Document Number Bandon / NorthBay 13" Rev X00

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DDR4 ball type: NON- Interleaved Type



[illegible]

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>CPU_(RESERVED)</i>			
Size A4	Document Number <i>Bandon / NorthBay 13"</i>		Rev <i>X00</i>
Date: Friday, February 15, 2019		Sheet 6 of	106

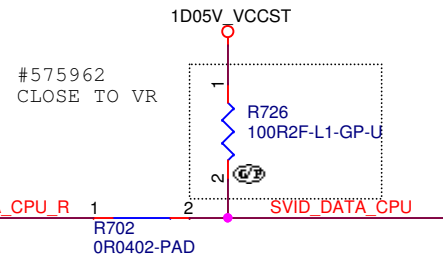
Main Func = CPU

Layout Note:

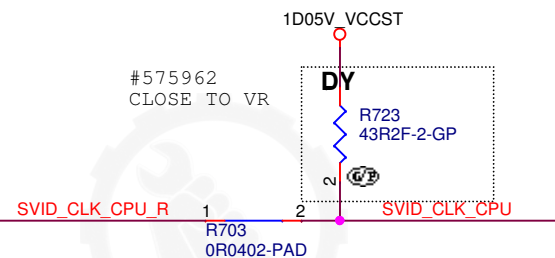
The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
Route the Alert signal between the Clock and the Data signals.

Vinafix.com

SVID DATA



SVID CLOCK



SVID ALERT

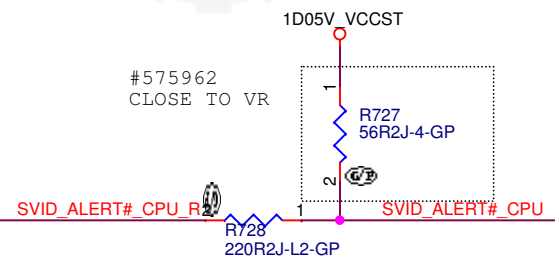
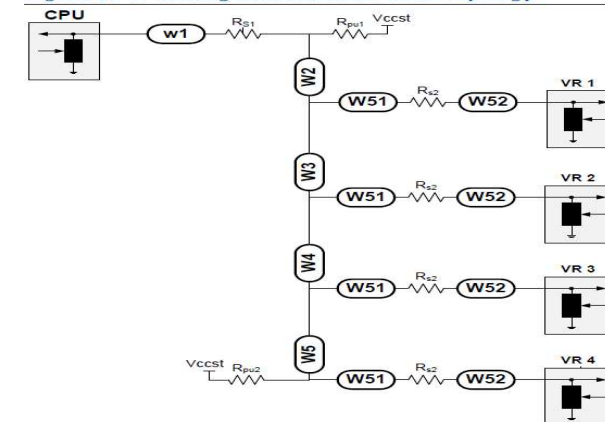


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{bus} [Ω]	R _{bus} [Ω]	R _{bus} [Ω]	R _{bus} [Ω]	W _{CPU} [inches]
VIDSOUT											
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	
VIDALERT#							Empty	45	0	50	1.0

Figure 10-7. Routing Illustration for SVID Topology



[46] VCCCORE_SENSE <<<<
[46] VSSCORE_SENSE <<<<
[46] SVID_DATA_CPU <<<<
[46] SVID_CLK_CPU <<<<
[46] SVID_ALERT#_CPU <<<<

1V_CPU_CORE CPU1L 12 OF 20 1V_CPU_CORE

AN9 VCCCORE VCCCORE AW24
AN10 VCCCORE VCCCORE AW25
AN24 VCCCORE VCCCORE AW26
AN26 VCCCORE VCCCORE AW27
AN27 VCCCORE VCCCORE AY24
AP2 VCCCORE VCCCORE AY26
AP9 VCCCORE VCCCORE BA5
AP24 VCCCORE VCCCORE BA7
AP26 VCCCORE VCCCORE BA8
AR5 VCCCORE VCCCORE BA25
AR6 VCCCORE VCCCORE BA27
AR7 VCCCORE VCCCORE BB2
AR8 VCCCORE VCCCORE BB26
AR10 VCCCORE VCCCORE BC5
AR25 VCCCORE VCCCORE BC6
AR27 VCCCORE VCCCORE BC7
AT9 VCCCORE VCCCORE BC9
AT24 VCCCORE VCCCORE BC10
AT26 VCCCORE VCCCORE BC26
AU5 VCCCORE VCCCORE BC27
AU6 VCCCORE VCCCORE BD5
AU7 VCCCORE VCCCORE BD8
AU8 VCCCORE VCCCORE BD10
AU9 VCCCORE VCCCORE BD25
AU24 VCCCORE VCCCORE BD27
AU25 VCCCORE VCCCORE BE9
AU26 VCCCORE VCCCORE BE24
AU27 VCCCORE VCCCORE BE25
AV2 VCCCORE VCCCORE BE26
AV5 VCCCORE VCCCORE BE27
AV7 VCCCORE VCCCORE BF2
AV10 VCCCORE VCCCORE BF9
AV27 VCCCORE VCCCORE BF24
AW5 VCCCORE VCCCORE BF26
AW6 VCCCORE VCCCORE BG27
AW7 VCCCORE VCCCORE
AW8 VCCCORE VCCCORE
AW9 VCCCORE VCCCORE
AW10 VCCCORE VCCCORE

VCC_SENSE AN6 VCCCORE_SENSE
VSS_SENSE AN5 VSSCORE_SENSE

VIDALERT# AA3 SVID_ALERT#_CPU_R

VIDSCK AA1 SVID_CLK_CPU_R

VIDSOUT AA2 SVID_DATA_CPU_R

RSVD#Y3 Y3

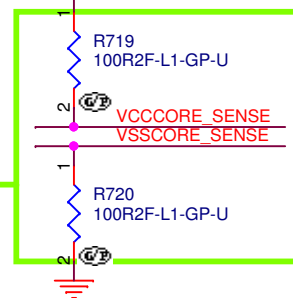
VCCSTG BG3



WHISKEY-LAKE-GP
ZZ.00CPU.271

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil



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Title

CPU(VCC CORE)

Size
A4

Document Number

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X00

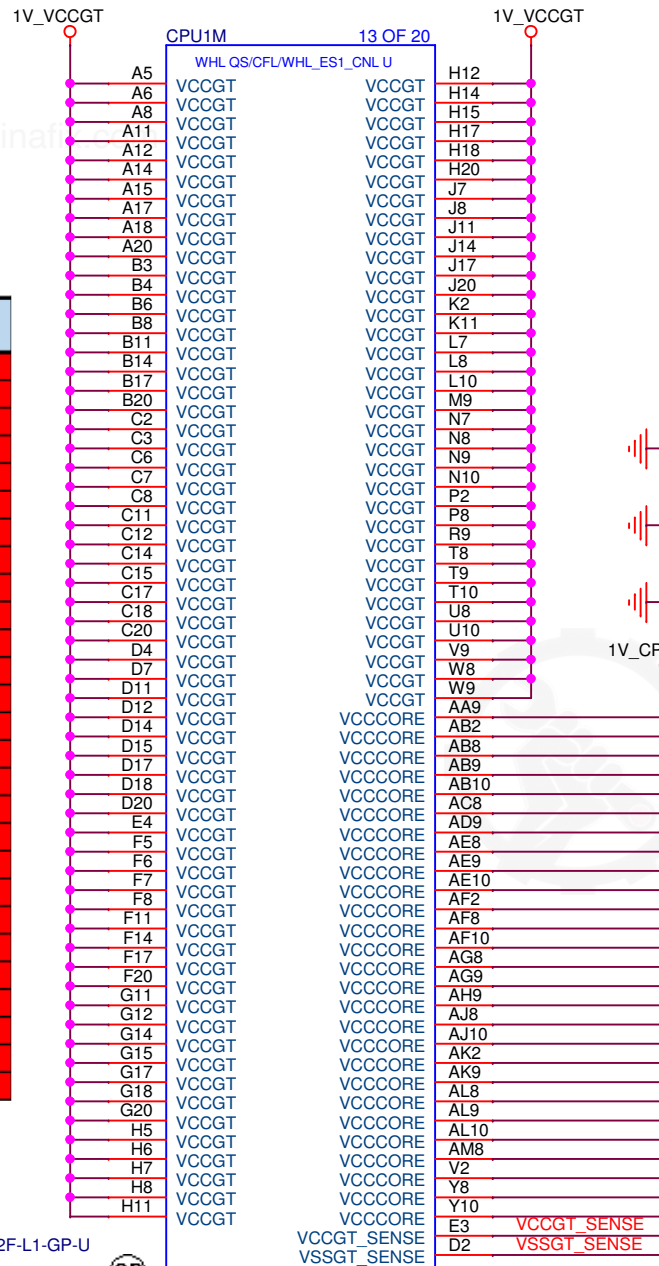
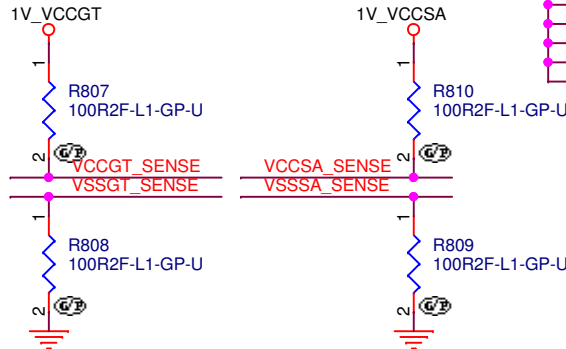
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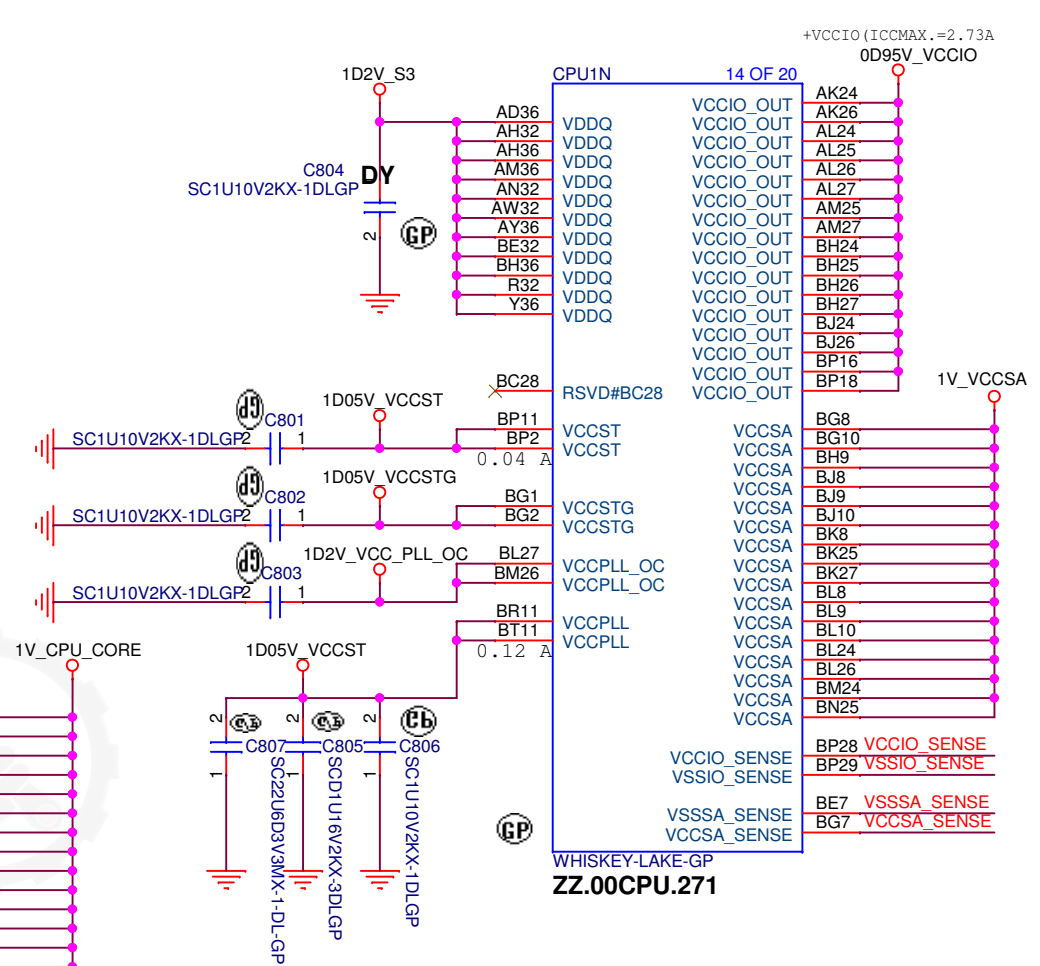
Main Func = CPU

[46] VCCGT_SENSE <<<< —
[46] VSSGT_SENSE <<<< —
[46] VSSA_SENSE <<<< —
[46] VCCSA_SENSE <<<< —
[54] VCCIO_SENSE >>>> —
[54] VSSIO_SENSE >>>> —

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



WHISKEY-LAKE-GP
ZZ.00CPU.271



WHISKEY-LAKE-GP
ZZ.00CPU.271

VCCPLL_OC	1x 1uF 0402		Do not merge VccPLL, VccPLL_OC and VccST to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VccPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		Placeholder Only. Can be placed on as either Primary or back side cap.
VccST	1x 1uF 0402		
VccSTG	1x 1uF 0402		

<Core Design>



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Title			CPU (DISPLAY)	
Size	Document Number	Bandon / NorthBay 13"		Rev
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Date: Friday, February 15, 2019		Sheet	8	of 106

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Title
(Reserved)

Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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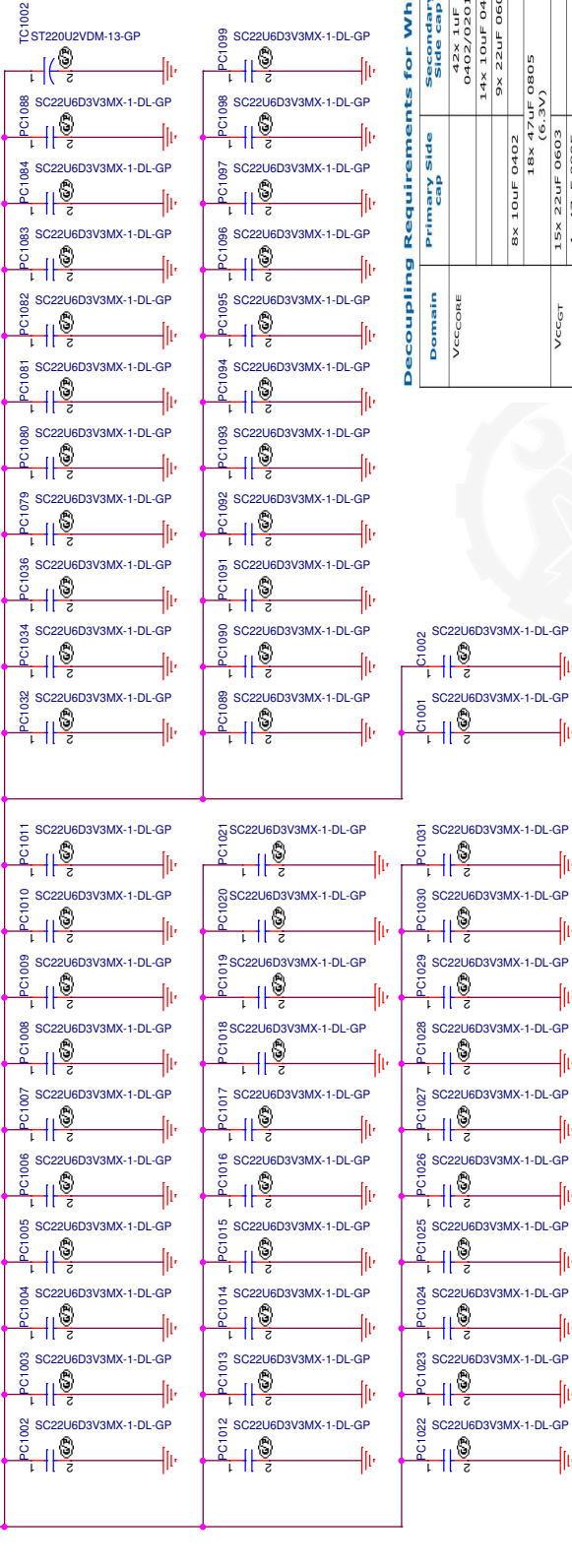
Date: Friday, February 15, 2019 Sheet 9 of 106

Main Func = CPU

Follow RO13 CAP account and vaule .

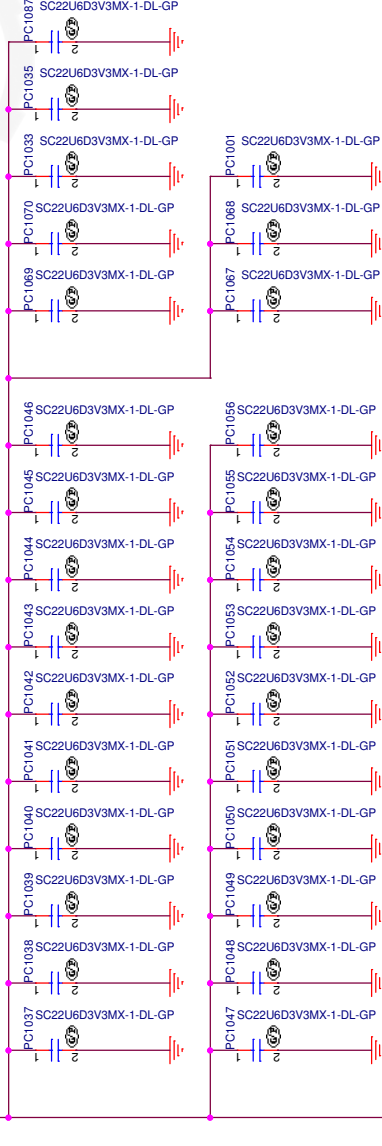
1V_CPU_CORE

220*52/2200*1
1V_CPU_CORE



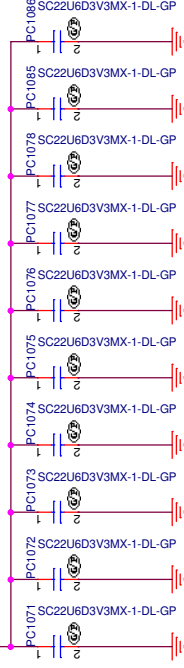
1V_VCCGT

220 x 38
1V_VCCGT



1V_VCCSA

220 x 10
1V_VCCSA



Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201 14x 10uF 0402 9x 22uF 0603	To be placed as close as possible to the vias that connect to the BGA pins.
VCCGT		18x 47uF 0805 (6.3V) 15x 22uF 0603 (6.3V) 4x 47uF 0805 (6.3V)	Place as close to the package as possible Place as close to the package as possible. Can be placed on as either Primary or back side cap. Place as close to the package as possible
		11x 1uF 0402/0201 15x 10uF 0402	Place as close to the package as possible

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCSA		4x 0402 7x 10uF 0402 6x 10uF 0402 2x 47uF 0805 (6.3V) 2x 0805	Placeholder only. Placeholder Only

Whiskey Lake U 4+2/Whiskey Lake U 4+2/Cannon Lake U 2+2/ Coffee Lake U 4+3e Bulk Decoupling Example

Bulk Decoupling Location	Example WHL U42	Example WHL U42F	Example CFL U43e	Notes
VCCORE Power VR	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	Placed at primary side output
VCCSA Power VR	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	Placed at primary side output
VCCGT Power VR	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	Placed at primary side output

Notes:
1. These examples are based on 1414Hz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR placement. Designers are recommended to consult with their VR vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

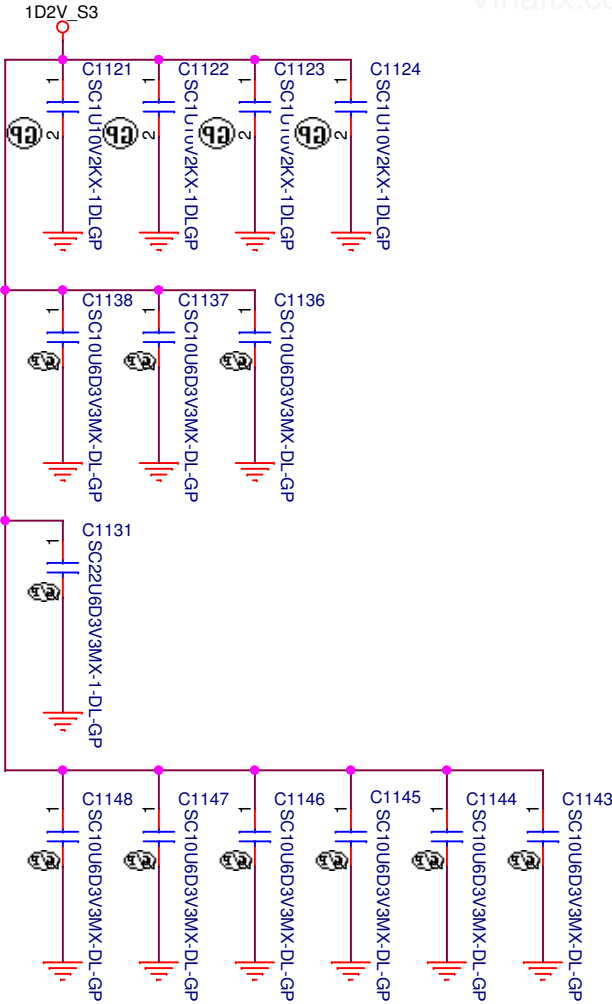
DELL
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CPU (Power CAP1)

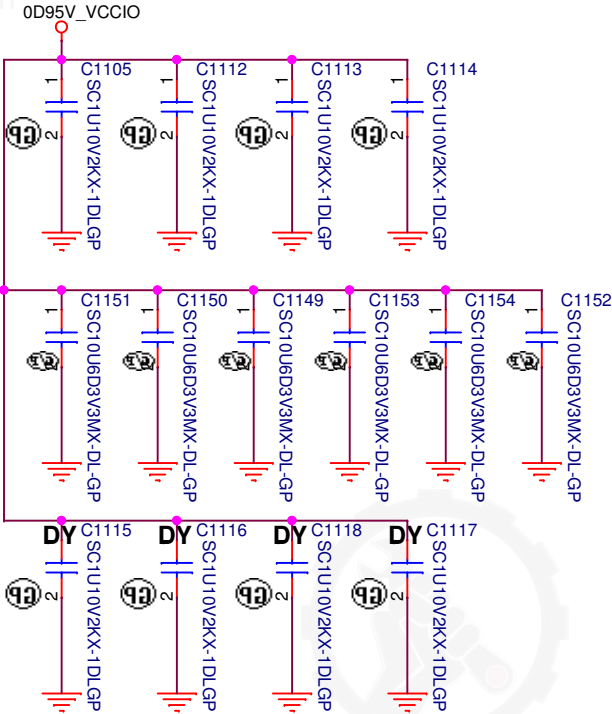
Size A3
Document Number Bandon / NorthBay 13"
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Sheet 10 of 106

Main Func = CPU

VDDQ




VCCIO



V _{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V _{CCIO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		Placeholder Only

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Title

CPU (Power CAP2)

Size
A4

Document Number
Bandon / NorthBay 13"

Rev
X00

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[5] M_A_A1[16:0] >>> M_A_A0
[5] M_A_A1
[5] M_A_A2
[5] M_A_A3
[5] M_A_A4
[5] M_A_A5
[5] M_A_A6
[5] M_A_A7
[5] M_A_A8
[5] M_A_A9
[5] M_A_A10
[5] M_A_A11
[5] M_A_A12
[5] M_A_A13
[5] M_A_A14
[5] M_A_A15
[5] M_A_A16

[5] M_A_BA0 >>>
[5] M_A_BA1 >>>
[5] M_A_BA2 >>>
[5] M_A_BG1 >>>

[5] M_A_CLK0 >>>
[5] M_A_CLK60 >>>
[5] M_A_CLK1 >>>
[5] M_A_CLK41 >>>

[5] M_A_CKE0 >>>
[5] M_A_CKE1 >>>

[5] M_A_CS40 >>>
[5] M_A_CS41 >>>

[5] M_A_ODT0 >>>
[5] M_A_ODT1 >>>

[99] CPU_SMB_SDA_DDR >>>
[99] CPU_SMB_SCL_DDR >>>

[5,13] SM_DRAMRST# >>>

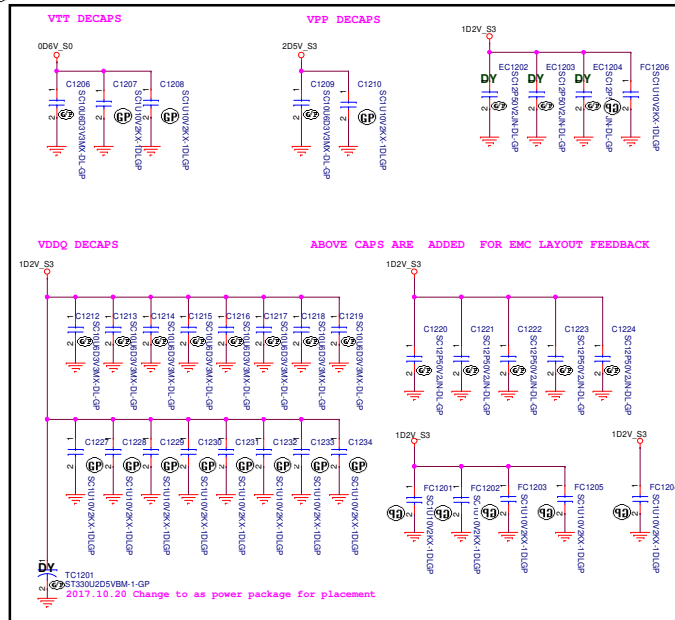
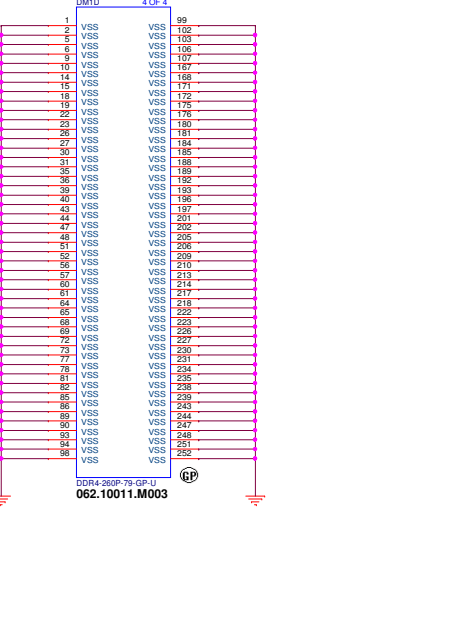
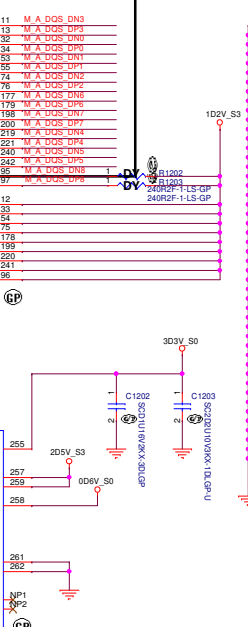
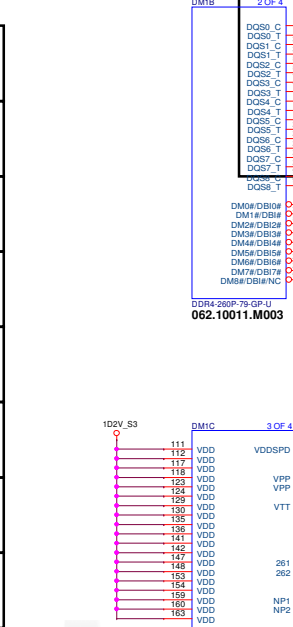
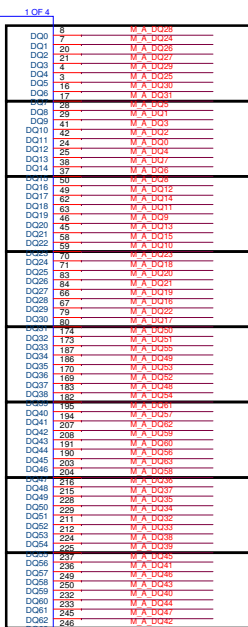
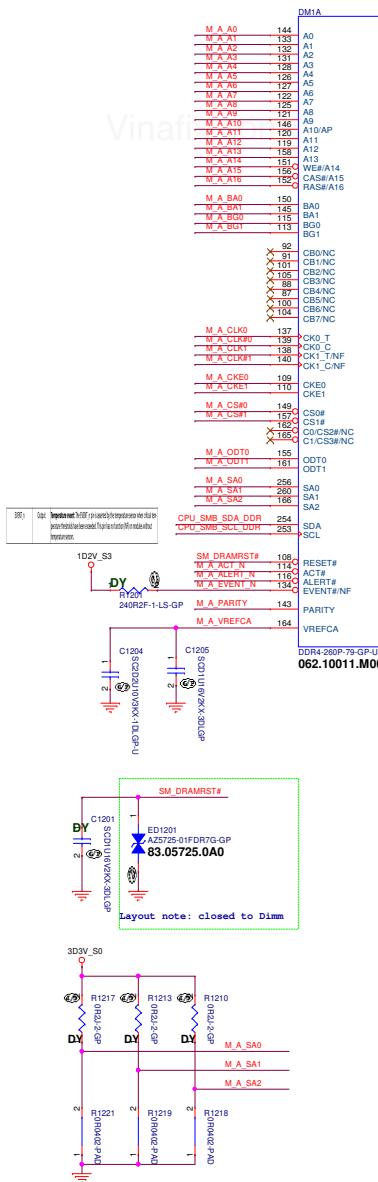
[5] M_A_ACT_N >>>
[5] M_A_ALERT_N >>>
[5] M_A_PARITY >>>

[5] M_A_DQ[83:0] <<< M_A_DQ0
[5] M_A_DQ1
[5] M_A_DQ2
[5] M_A_DQ3
[5] M_A_DQ4
[5] M_A_DQ5
[5] M_A_DQ6
[5] M_A_DQ7
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[5] M_A_DQ63

M_A_DQS_DN[7:0] <<< M_A_DQS_DN0
[5] M_A_DQS_DN1
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[5] M_A_DQS_DN5
[5] M_A_DQS_DN6
[5] M_A_DQS_DN7

M_A_DQS_DP[7:0] <<< M_A_DQS_DP0
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[5] M_A_DQS_DP5
[5] M_A_DQS_DP6
[5] M_A_DQS_DP7

```



WHL-U DDR4 SODIMM Decoupling

This recommendation assumes a 2CH, 1DPC (2 connector) implementation of SO DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μF (size)
DDR4 SODIMM 10Rx8	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10μF (6603)
		4 near each side of the DIMM connector close to VDD pins	16x 1μF (0402)
	VTT	Place on VTT plane close to SODIMM 1 cap, supported, 1 placholator	2x 330μF (2343)
		Place on VTT plane close to SODIMM	2x 10μF (6603)
	VPP	DIMM pin side, 1 per DIMM	4x 1μF (0402)
		DIMM pin side, 1 per DIMM	2x 10μF (6603)
	VDDSDPD	Place close to DIMM	2x 0.1μF (0402)
		Place close to DIMM	2x 2.2μF (0402)

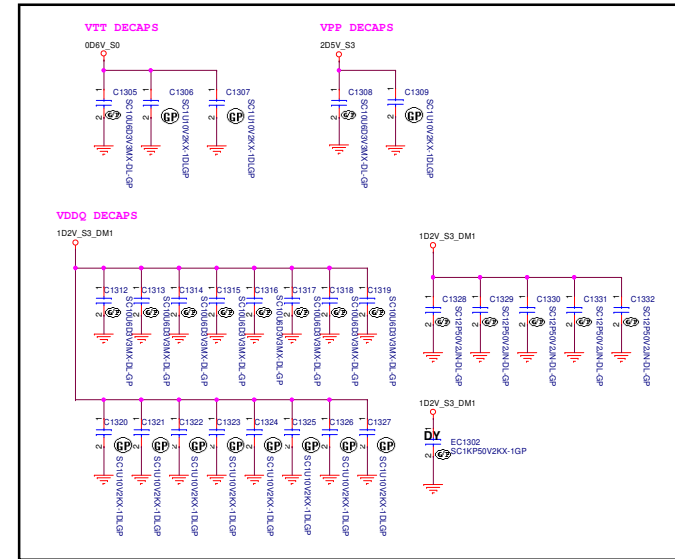
Notes:

Core Design:



Title DDR (DDR4-CHA)			
Size A2	Document Number Bandon / NorthBay 13"	Rev X00	
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[5] V_SM_VREF_CNTB >>>_____



Title			
DDR (DDR4-CHB)			
Size A2	Document Number	Rev	
	Bandon / NorthBay 13"	X00	
Date:	Friday, February 15, 2019	Sheet 13 of	106

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Title
(Reserved)_SODIMM _SODIMM4

Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Date: Friday, February 15, 2019 Sheet 14 of 106

Main Func = PCH

[19.27] SPKR <<<-
[20] NR_B BIT <<<-
[18.68.99] SPI_SL_CPU <<<-
[18.68.99] SPI_WP_CPU <<<-
[18.68.99] SPI_HOLD_CPU <<<-
[18] GPP_C2 <<<-
[6.99] CFG3 <<<-
[6.99] CFG4 <<<-
[15.21] GPD_7 <<<-

[20] GPP_D12 >>>-
[18] GPP_B23 >>>-
[15.21] GPD_7 >>>-
[21] GPP_H21 >>>-
[21] GPP_H23 >>>-
[6.99] ITP_PMODE >>>-
[19] HDA_SDO >>>-
[18] GPP_C5 >>>-
[20] GPP_B22 >>>-
[20.61] CNV_RGL_DT >>>-

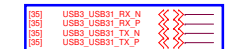
Description	Top Swap Override	No Reboot	TLS Confidentiality	BOOT BIOS STRAP (BBS)	ESPI OR LPC	BOOT HALT
GPIO	GPP_B14 / SFER / TIME_SYNC1 / GSP10_CS#	GPP_B18	GPP_C2	GPP_B22	GPP_C5	SPI0_MOSI
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	SPI SELECTED. (DEFAULT)	LPC SELECTED	
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	LPC SELECTED FOR SYSTEM FLASH	HIGH: ESPI IS SELECTED FOR EC	This strap should sample HIGH.
	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-up.

Description	JTAG ODT DISABLE	EXI BOOT STALL BYPASS	CONSENT STRAP	A0 PERSONALITY STRAP	Flash Descriptor Security Override	DFXTESTMODE
GPIO	GPP_D12	GPP_B23	SPI0_IO2	SPI0_IO3	HDA_SDO/12S0_TXD	ITP_PMODE
LOW	JTAG ODT DISABLED	ENABLED (BSSB 2+2)	ENABLED	ENABLED	Enable security measures, and security is not overridden	DFXTESTMODE DISABLE (DEFAULT)
HIGH	JTAG ODT ENABLED	DISABLED (BSSB 4 WIRE)	DISABLED	DISABLED	Disable security measures, and security is overridden	DFXTESTMODE ENABLE
	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-down.	20 K± 30% internal pull-up

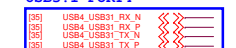
Description	RING OSCILLATOR BYPASS	XTAL FREQUENCY SELECT	M.2 CNVi Mode Select	MAF/SAF STRAP
GPIO	GPD7	GPP_H21	GPP_F6 / CNV_RGL_DT	GPP_H23
LOW	XTAL INPUT IS SINGLE ENDED	38.4/19.2MHZ (DEFAULT)	Integrated CNVi enabled	MAF ENABLE
HIGH	XTAL INPUT IS ATTACHED	24MHZ	Integrated CNVi disabled	SAF ENABLE

Main Func = PCH

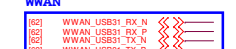
USB3.1 PORT3



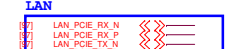
USB3.1 PORT4



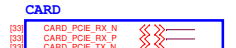
WWAN



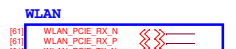
LAN



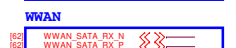
CARD



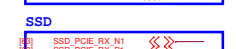
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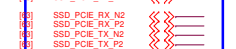
SSD



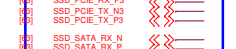
Type C port 1



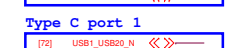
FP



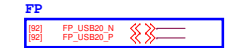
USB charger



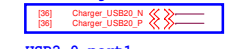
USB2.0 port1



CAMERA



WWAN



USH



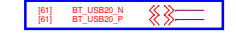
BT



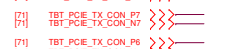
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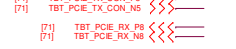
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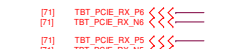
BT



BT



BT



BT



BT



#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.



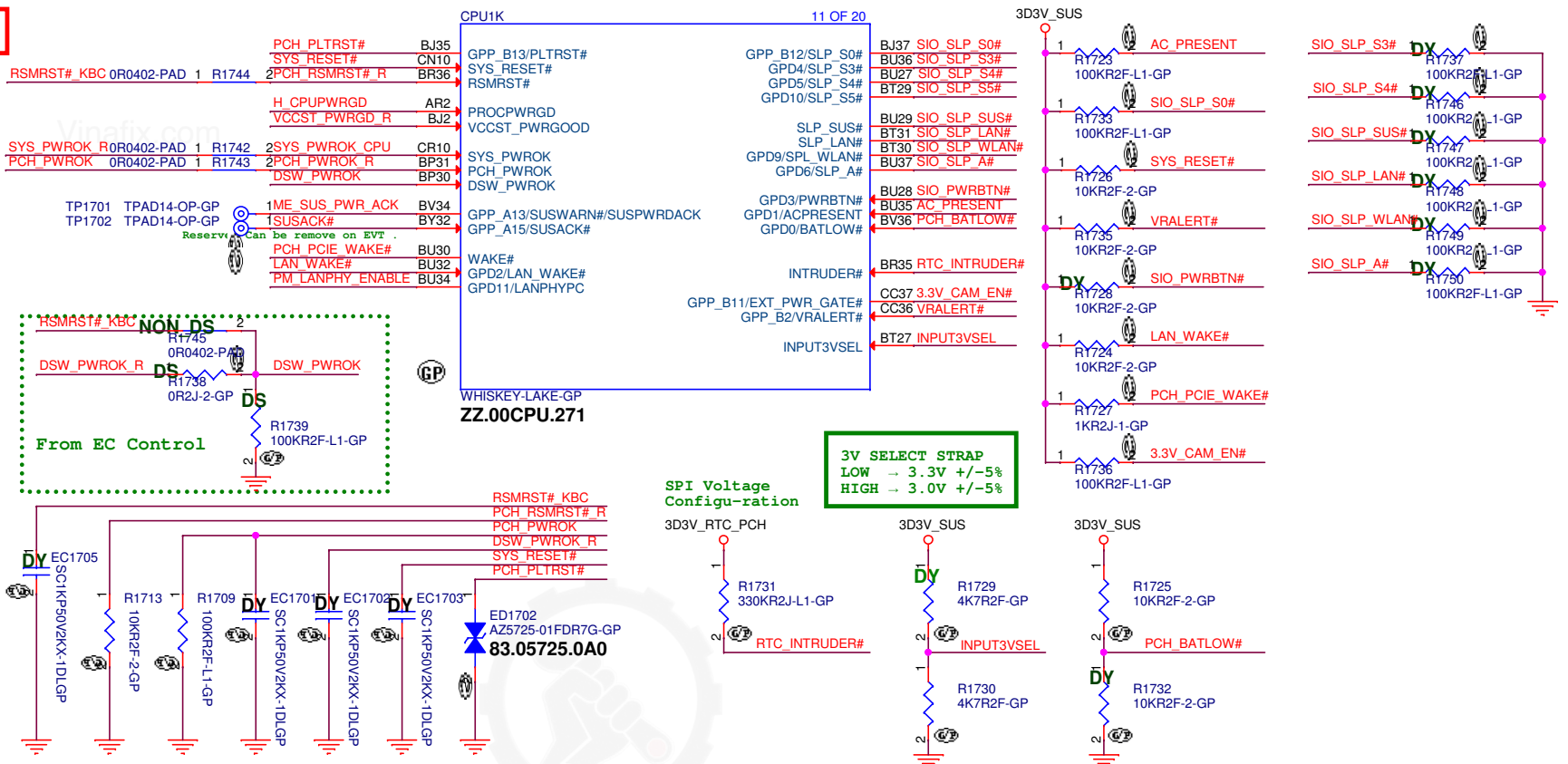
Layout Note:

- 1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
- Note: Must maintain low DC resistance routing (<0.1 ohm).
- 2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

		PCIe Controller 1				PCIe Controller 2				PCIe Controller 3				PCIe Controller 4			
		SATA Port 1 can be mapped to HSD 12 or 15															
		PCIe Gen3 (8 CLKS)															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Canoe Lake U PCHLP		USB1.1/13.0	USB2.1/13.0	USB3.1/13.0	USB5.1/13.0	USB1.1/13.0	USB2.1/13.0	GfE	GfE	GfE	PCH-10	SATA0	SATA-1	GfE	GfE	SATA-1*	SATA2
		-1	2	-3	-4	-5	-6					PCH-11	PCH-12	PCH-13	PCH-14	PCH-15	PCH-16
		X.2		X.2		X.2		X.2		X.2		X.2		X.2		X.2	
		X.4				X.4				X.4				X.4			
		No Remapping				No Remapping				Intel RST for PCIe Storage Device				Intel RST for PCIe Storage Device			
North Bay 13 Bandon	13 U0 (non-TBT)	Type-C Port1 (gen2)	Type-A Port1 (gen1)	Type-A Port2 (gen1)	M.2 3042 (LTE)					LOM	M.2 2230 (M.0AN)	SD Reader	M.2 3042 (LTE)	M.2 2230 (PCIe 4.0 or SATA SSD)		M.2 2230 (M.0AN)	
	13 U0 (TBT)	Type-A Port1 (gen1)	Type-A Port2 (gen1)	M.2 3042 (LTE)	TBT Controller x4				LOM	M.2 2230 (M.0AN)	SD Reader	M.2 3042 (LTE)	M.2 2230 (PCIe 4.0 or SATA SSD)		M.2 2230 (M.0AN)		

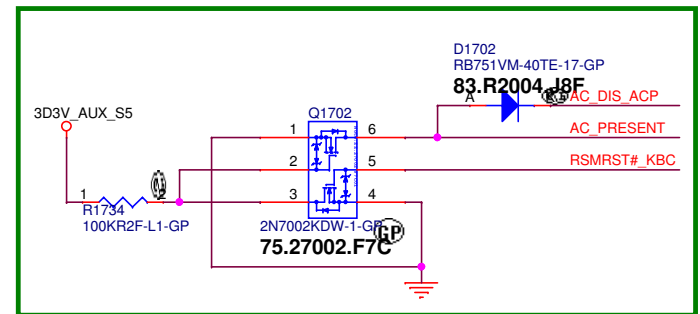
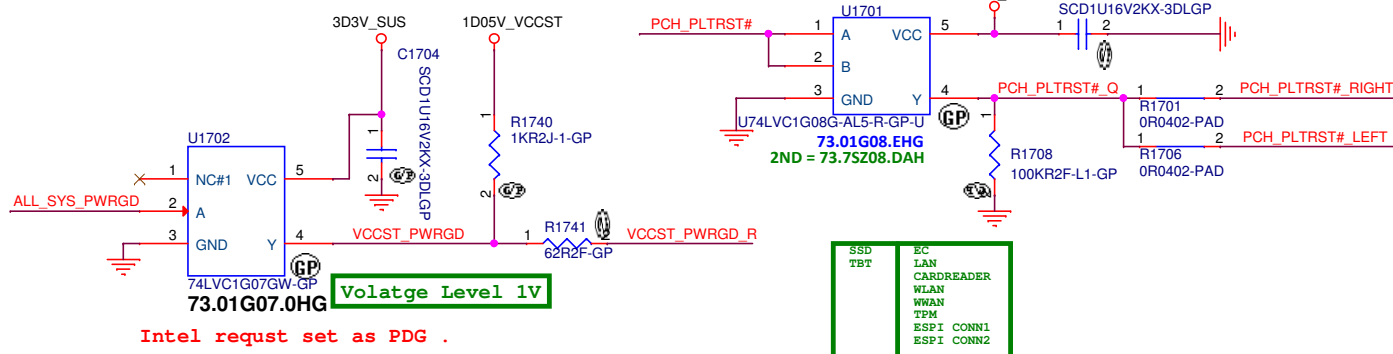
Main Func = PCH

[24,40,52,53,54]	SIO_SLP_SUS#	<<<<
[68]	SIO_SLP_S5#	<<<<
[40,51,68]	SIO_SLP_S4#	<<<<
[24,40,51,68,71]	SIO_SLP_S3#	<<<<
[68]	SIO_SLP_A#	<<<<
[40,54,68,91]	SIO_SLP_S0#	<<<<
[40]	SIO_SLP_WLAN#	<<<<
[40]	SIO_SLP_LAN#	<<<<
[68,99]	SYS_RESET#	<<<<
[24]	DSW_PWROK_R	<<<<
[46]	PCH_PWROK	<<<<
[24]	SYS_PWROK_R	<<<<
[24,99]	SIO_PWRBTN#	>>>>
[24]	AC_PRESENT	<<<<
[24,97]	LAN_WAKE#	<<<<
[24,62,71]	PCH_PCIE_WAKE#	<<<<
[97]	PM_LANPHY_ENABLE	<<<<
[18,24]	RTCST_ON	>>>>
[24,64,99]	RSMRST#_KBC	>>>>
[24]	ALL_SYS_PWRGD	>>>>
[33,61,62,91,97]	PCH_PLTRST#_RIGHT	<<<<
[63,71,99]	PCH_PLTRST#_LEFT	<<<<
[21,24,40,54,91]	CPU_C10_GATE#	<<<<
[3]	H_CPUPWRGD	<<<<
[40]	3.3V_CAM_EN#	>>>>
[44]	AC_DIS_ACP	>>>>



PCH_PWROK: pull-up resistance should be in range 1/10th of pull down resistance

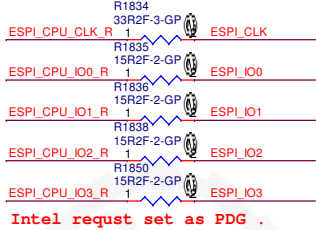
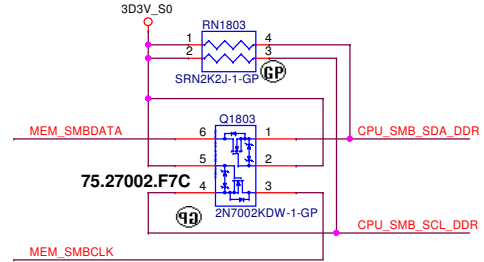
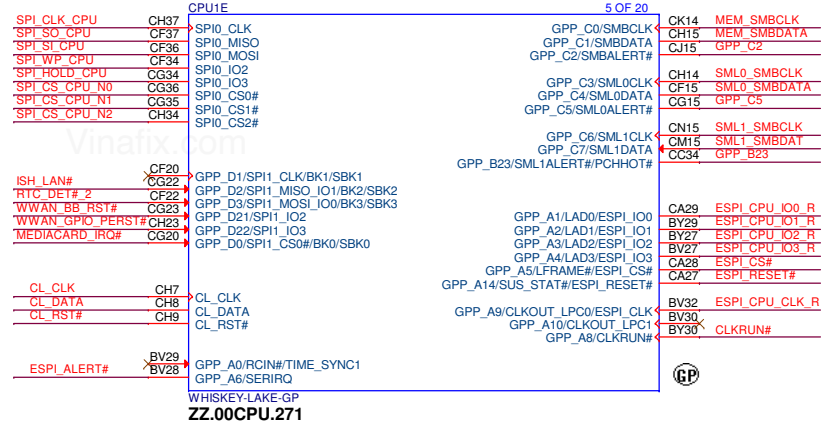
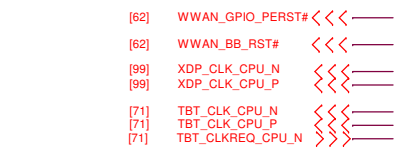
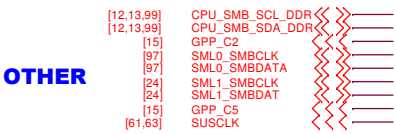
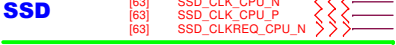
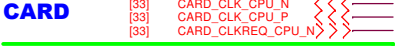
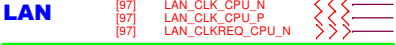
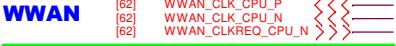
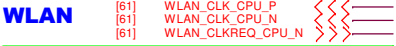
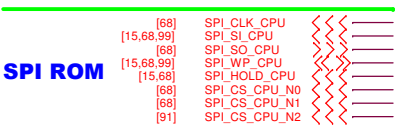
CheckList 10K , Reserve PL for RTC rst test



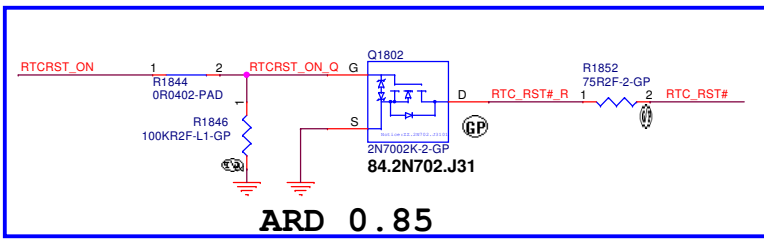
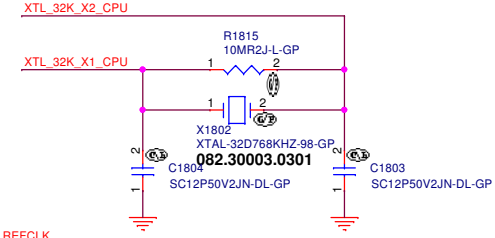
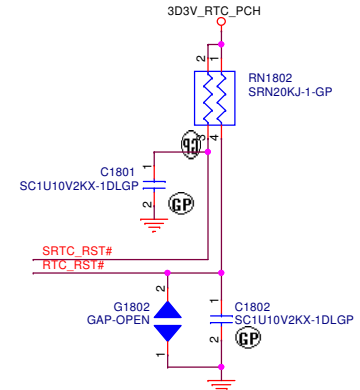
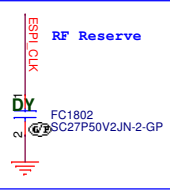
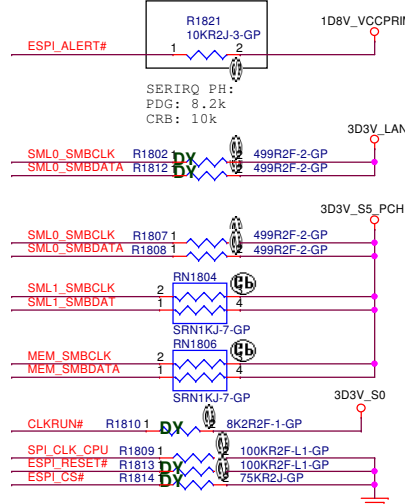
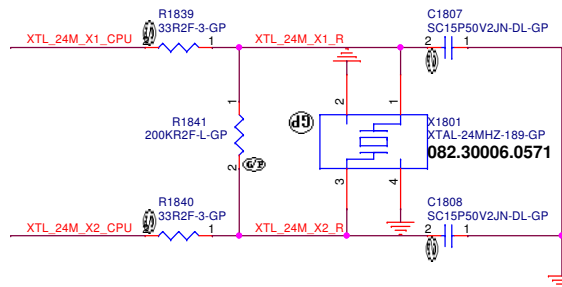
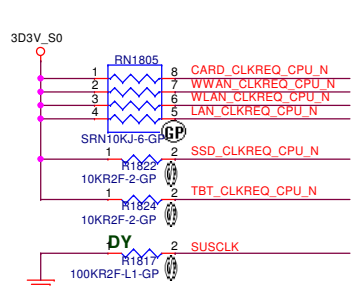
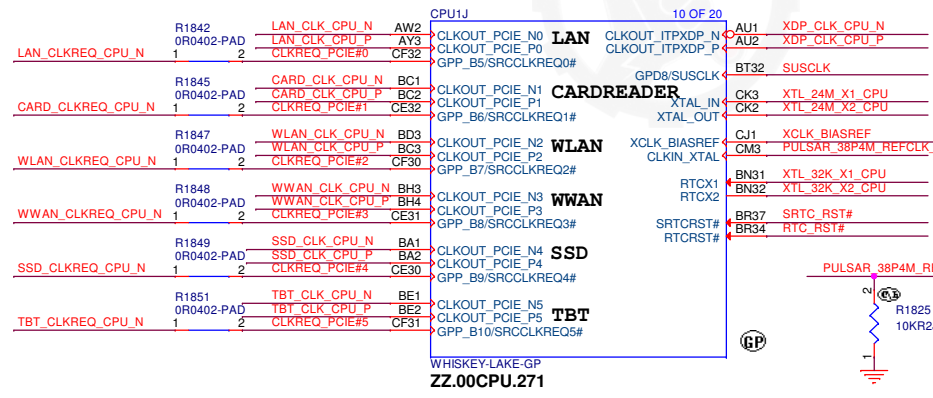
<Core Design>

DELL		Wistron Corporation	
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Title CPU_(POWER MANAGEMENT)			
Size Custom	Document Number	Rev X00	
Date: Friday, February 15, 2019		Sheet 17 of 106	

Main Func = PCH



Pin Name	System Pull-up/Pull-down	System Notes
ESPI_CLK	15.0k	ESPI_CLK is a 15.0k series resistor, placed near the driver for Data Signal Integrity. For Clock, placed near the driver. Note that ESPI_CLK and ESPI_RESET# do not require series resistors.



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DELL

CPU (LPC/SPI/SMBUS/CL/CLK)

Bandon / NorthBay 13"

Rev X00

Date: Friday, February 15, 2019

Sheet 18 of 106

Main Func = PCH

[27] HDA_SDIO <<< —
[27] HDA_SDOOUT_CODEC <<< —
[27] HDA_SYNC_CODEC <<< —
[27] HDA_BITCLK_CODEC <<< —
[15] HDA_SDO <<< —

[66] CONTACTLESS_DET# >>> —

[56] CAM_MIC_CBL_DET# >>> —

[29] SPK_DET# >>> —

[33] HOST_SD_WP# >>> —

[27] AUD_PWR_EN <<< —

[68] ME_FWP_PCH <<< —

[15,27] SPKR <<< —

[61] CLKREQ_CNV >>> —
[61] CNV_RF_RESET# >>> —

[65] KB_DET# <<< —

[62] WWAN_GPIO_WAKE# <<< —

[71] TBT_CIO_PLUG_EVENT# <<< —

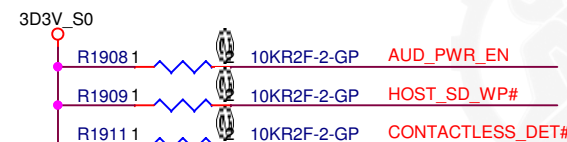
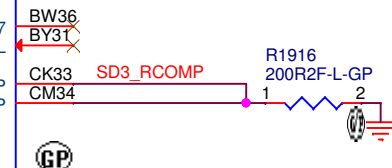
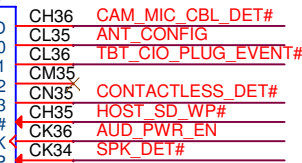
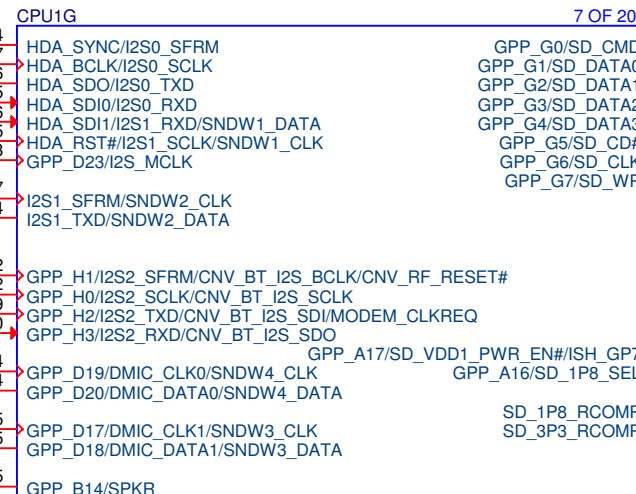
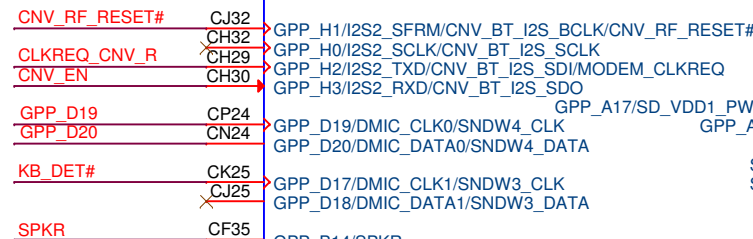
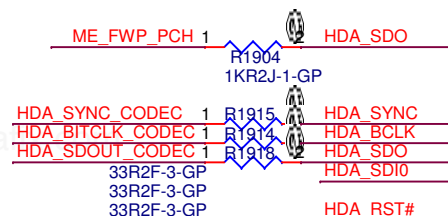
[56] DMIC_SDA_CODEC_CPU <<< —

[56] DMIC_SCL_CODEC_CPU <<< —

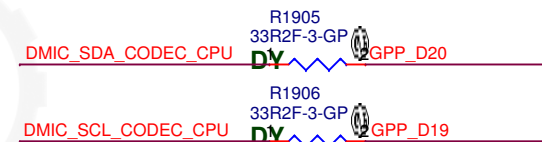
[62] ANT_CONFIG >>> —

[61] CNV_EN <<< —

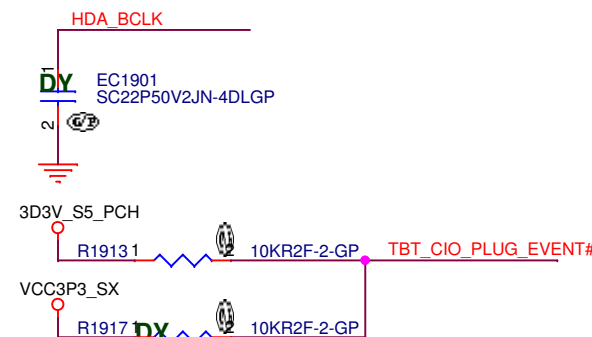
[27] HDA_RST# <<< —



GPI00.5 change to 1.8V



Reserve for Dmic connect to PCH



<Core Design>



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Title

CPU (AUDIO/SDIO/SDXC)

Size
A4

Document Number

Bandon / NorthBay 13"

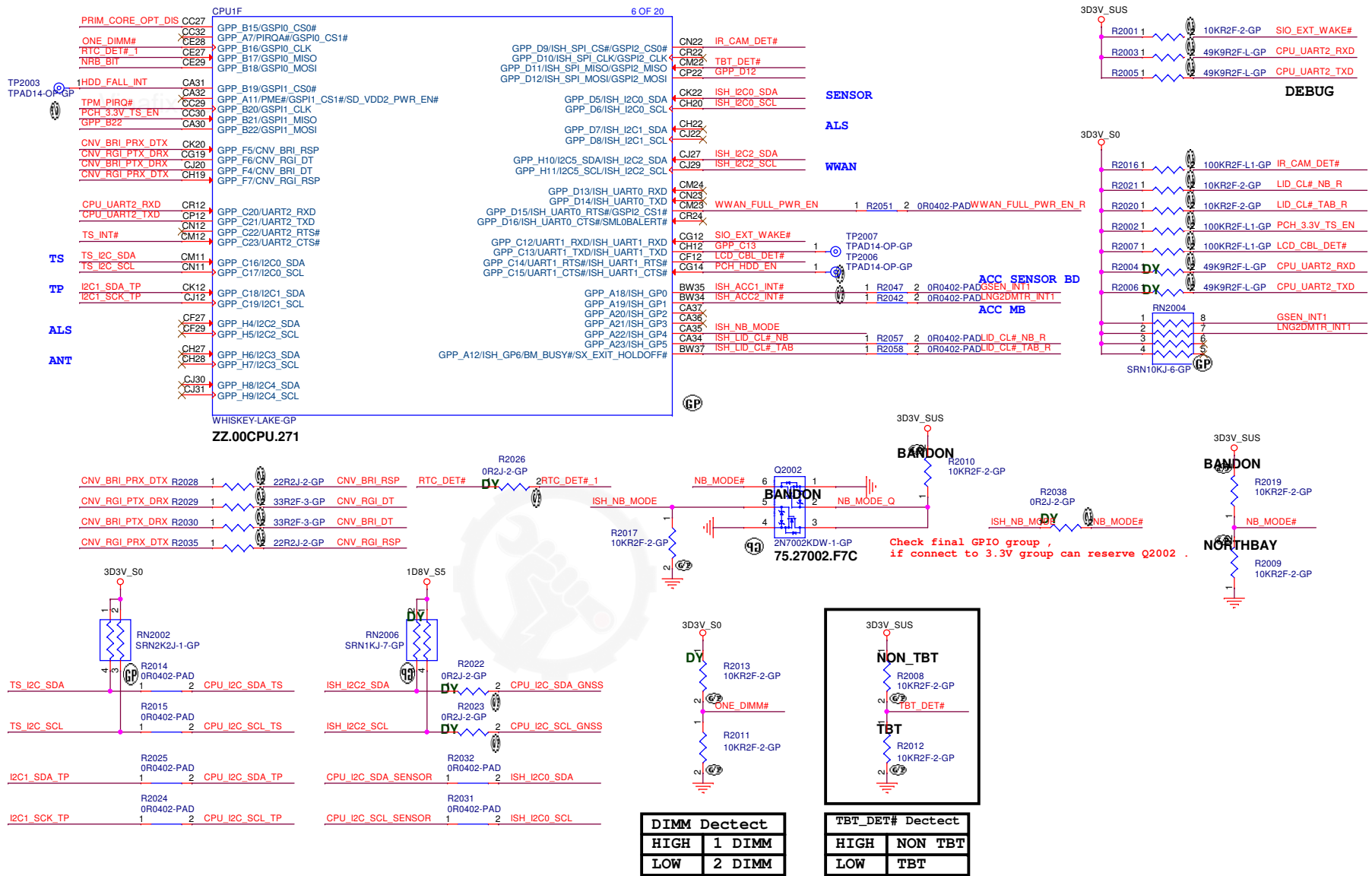
Rev
X00

Date: Friday, February 15, 2019

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Main Func = PCH

[68]	CPU_UART2_TXD	<<<
[68]	CPU_UART2_RXD	<<<
[55]	CPU_I2C_SDA_TS	<<<
[55]	CPU_I2C_SCL_TS	<<<
[65]	CPU_I2C_SDA_TP	<<<
[65]	CPU_I2C_SCL_TP	<<<
[69,70]	CPU_I2C_SDA_SENSOR	<<<
[69,70]	CPU_I2C_SCL_SENSOR	<<<
[62]	CPU_I2C_SDA_GNSS	<<<
[62]	CPU_I2C_SCL_GNSS	<<<
[69]	GSEN_INT1	<<<
[70]	LNG2DMTR_INT1	<<<
[24]	NB_MODE#	<<<
[24]	LID_CL#_NB_R	<<<
[24]	LID_CL#_TAB_R	<<<
[15,20]	NRB_BIT	<<<
[91]	TPM_PIRQ#	<<<
[40]	PCH_3.3V_TS_EN	<<<
[15]	GPP_B22	<<<
[55]	TS_INT#	<<<
[24]	SIO_EXT_WAKE#	<<<
[55]	LCD_CBL_DET#	<<<
[61]	CNV_BRI_RSP	<<<
[15,61]	CNV_RGI_DT	<<<
[61]	CNV_RGI_DT	<<<
[61]	CNV_RGI_RSP	<<<
[15,20]	NRB_BIT	<<<
[15]	GPP_D12	<<<
[56]	IR_CAM_DET#	<<<
[62]	WWAN_FULL_PWR_EN#	<<<
[54]	PRIM_CORE_OPT_DIS	<<<
[18,25]	RTC_DET#	<<<

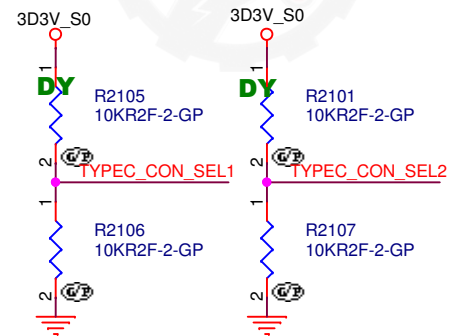
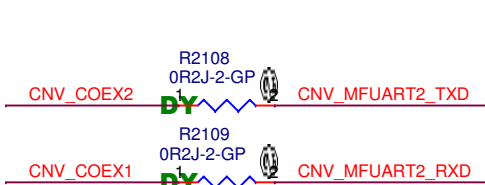
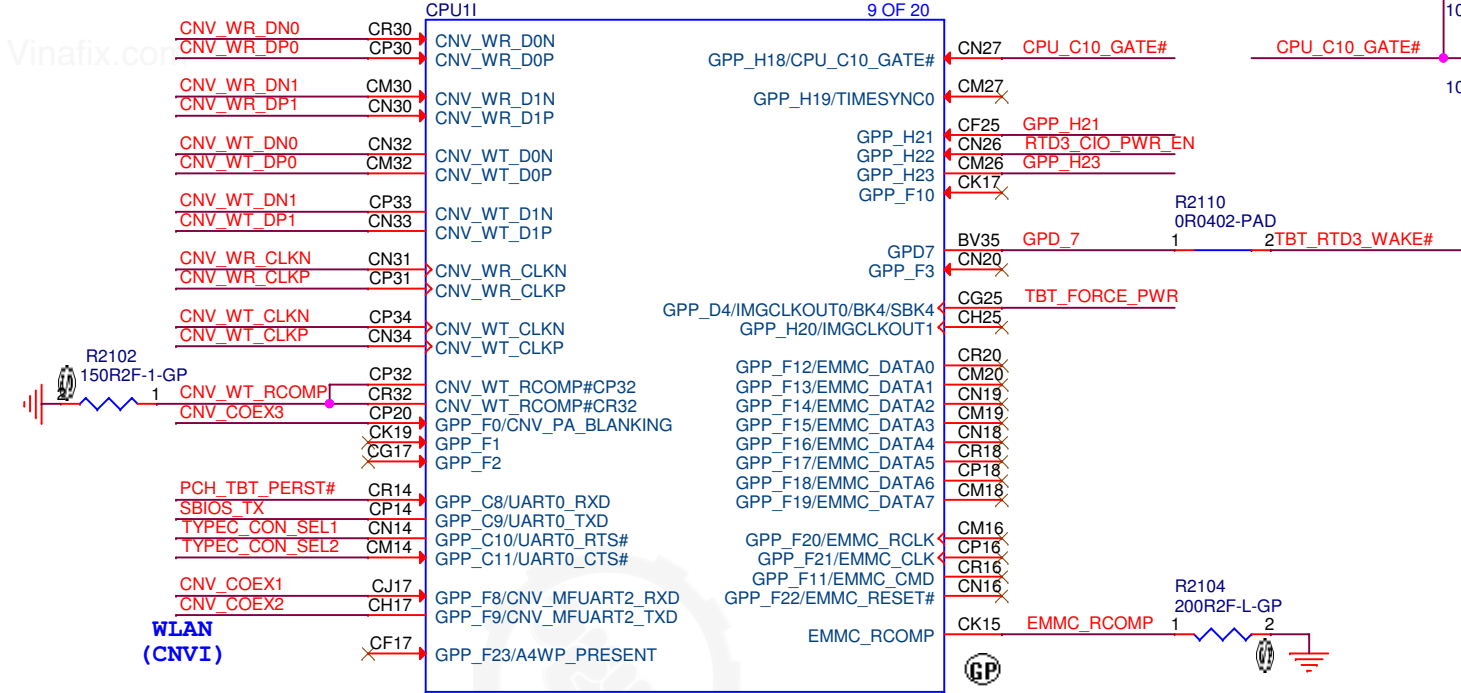
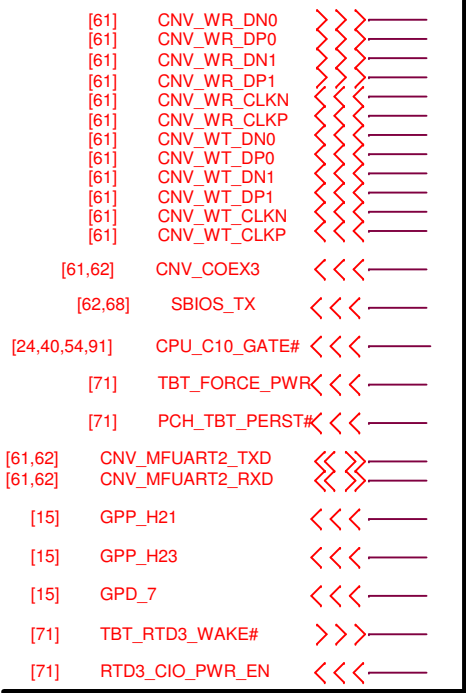


<Core Design>

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Title **CPU (LPSS/ISH)**
Size A3 Document Number **Bandon / NorthBay 13"** Rev **X00**
Date: Friday, February 15, 2019 Sheet 20 of 106

Main Func = PCH



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

<Core Design>



Wistron Corporation
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Title

CPU (POWER1)

Size
A4

Document Number
Bandon / NorthBay 13"

Rev
X00

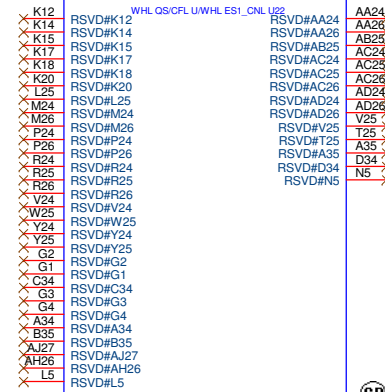
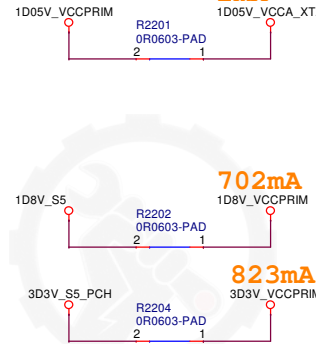
Date
Friday, February 15, 2019

Sheet
21

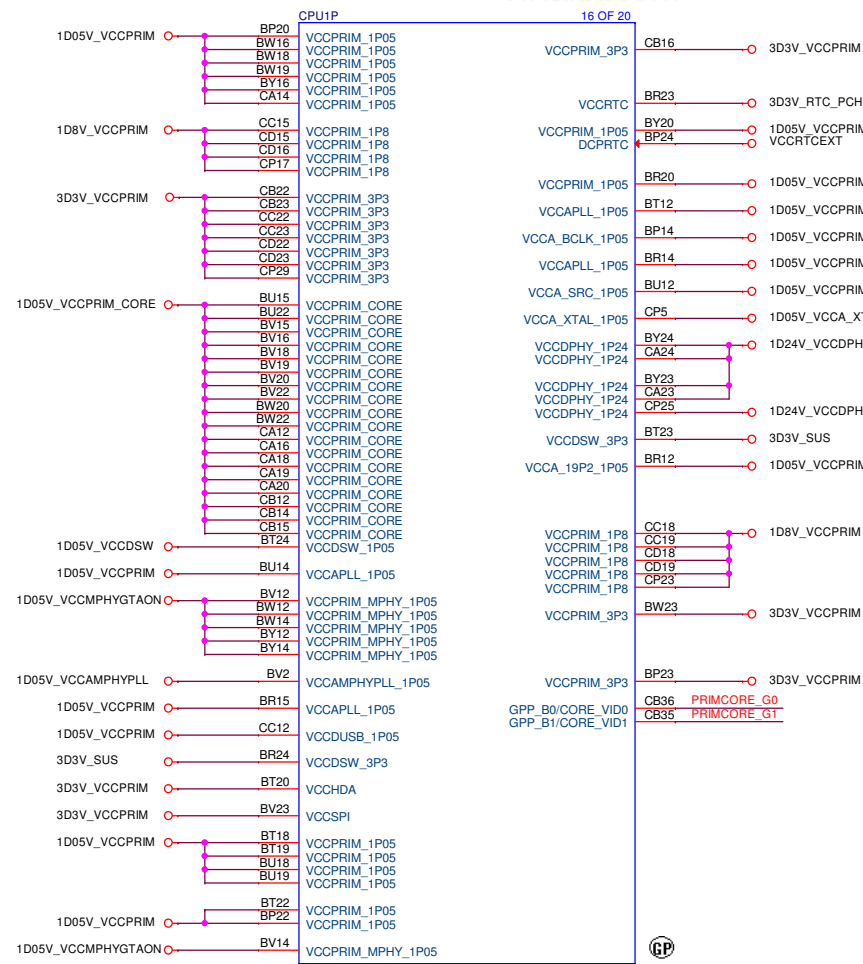
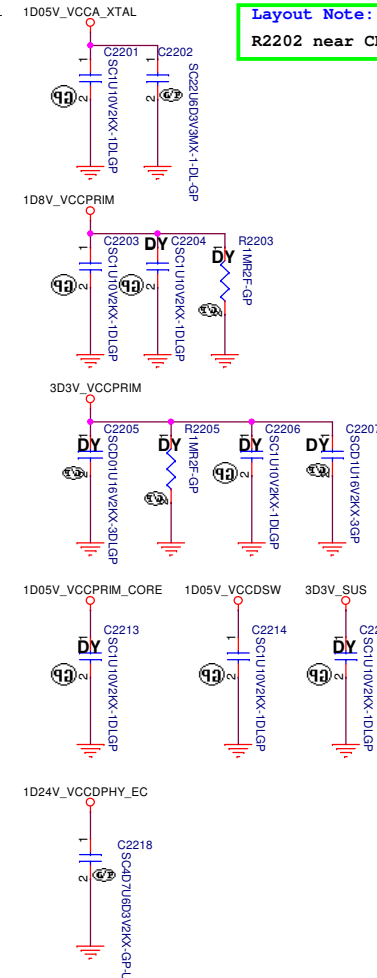
of
106

```
[54] PRIMCORE_G0    >>>_____
[54] PRIMCORE_G1    >>>_____
```

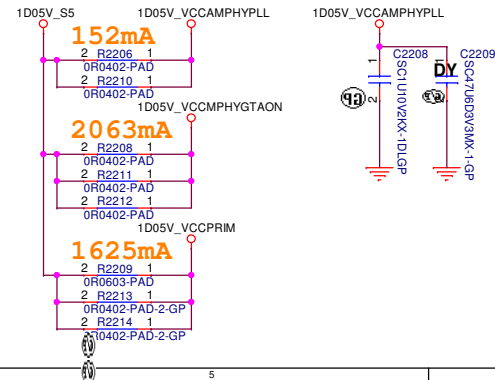
CPU10 15 OF 20

 $2m$ 

Layout Note:
R2202 near C



Layout Note:
22uF:
C2209 near B

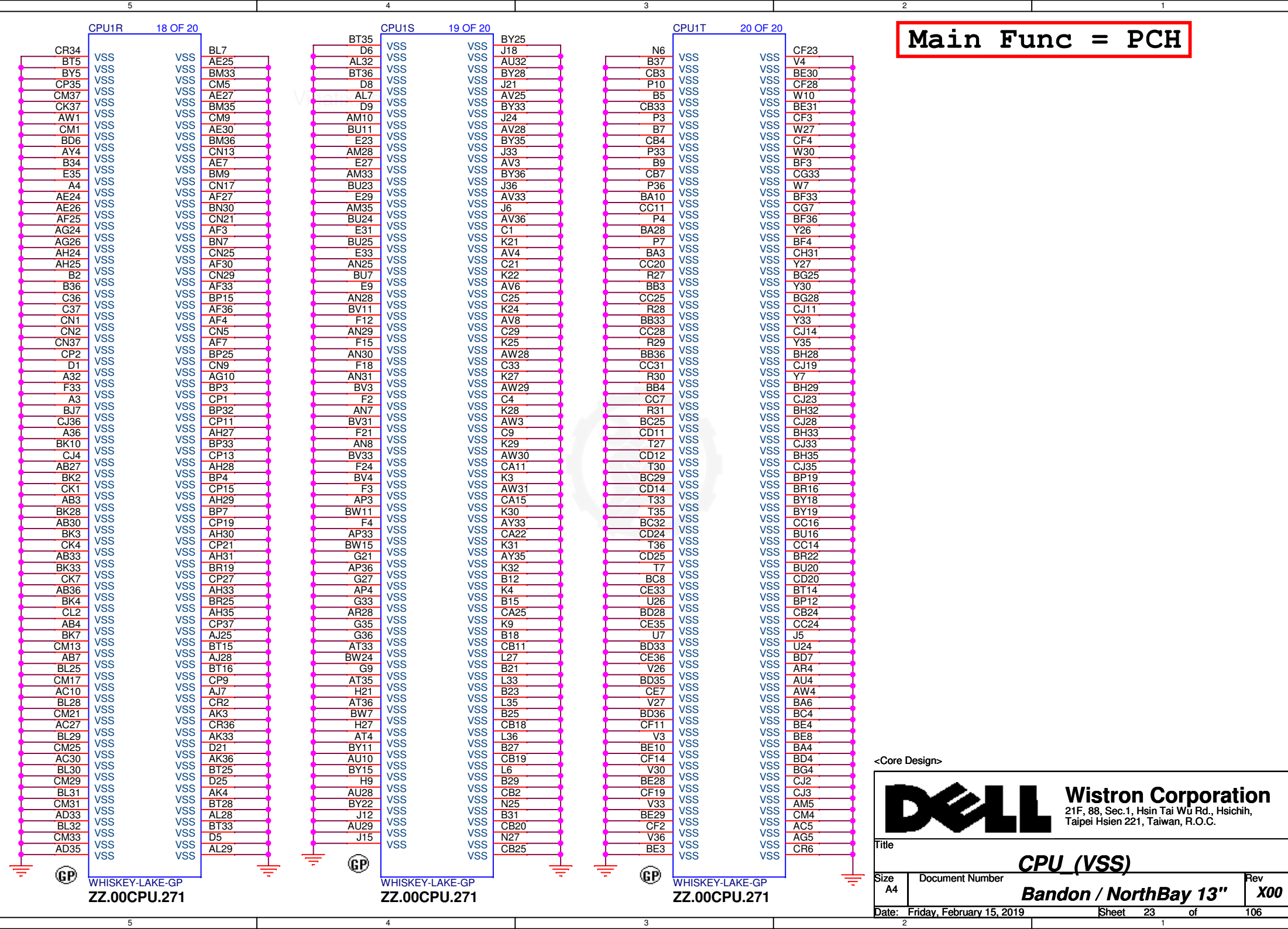


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Taipei Hsien 221, Taiwan, R.O.C.

CPU (RSVD)

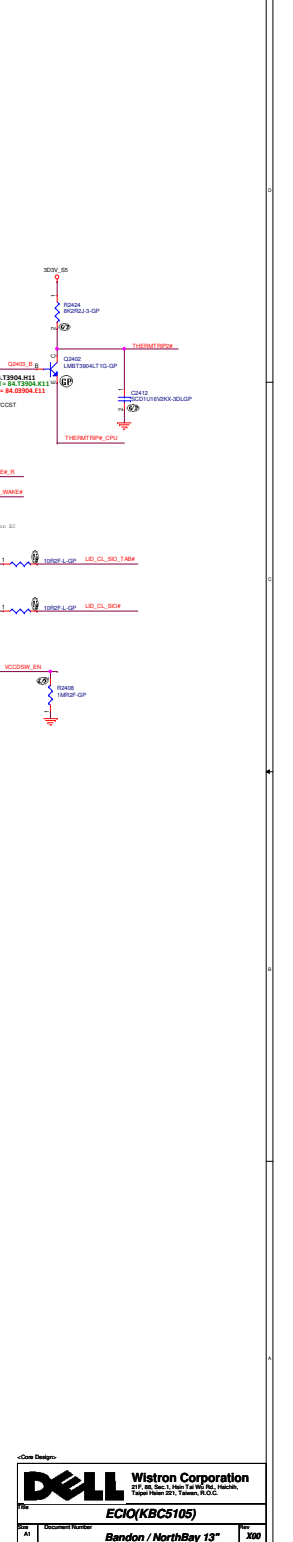
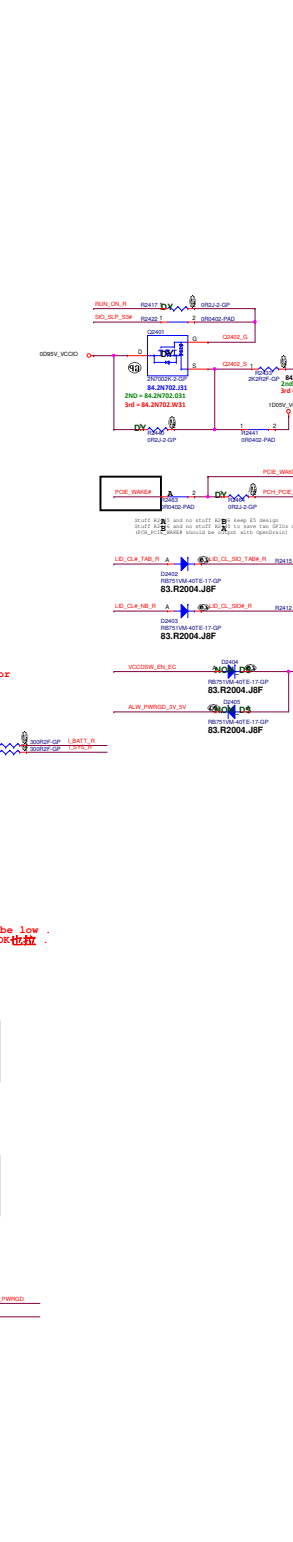
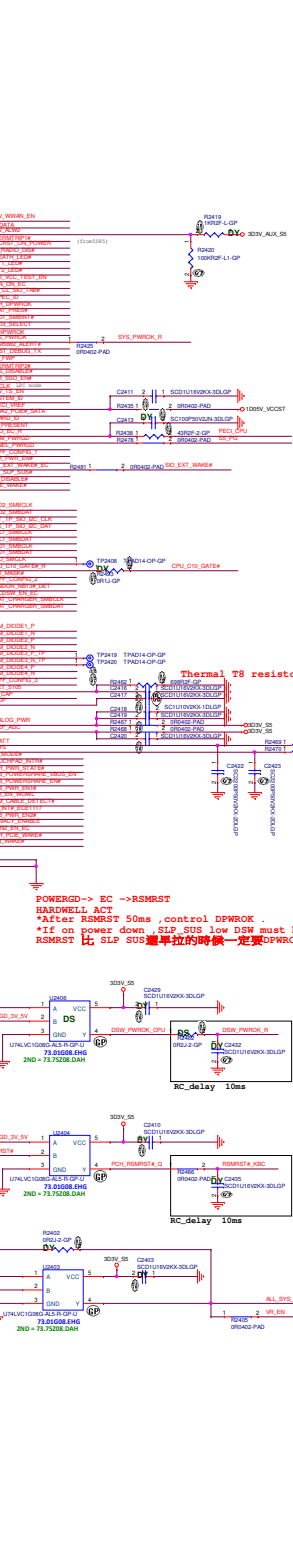
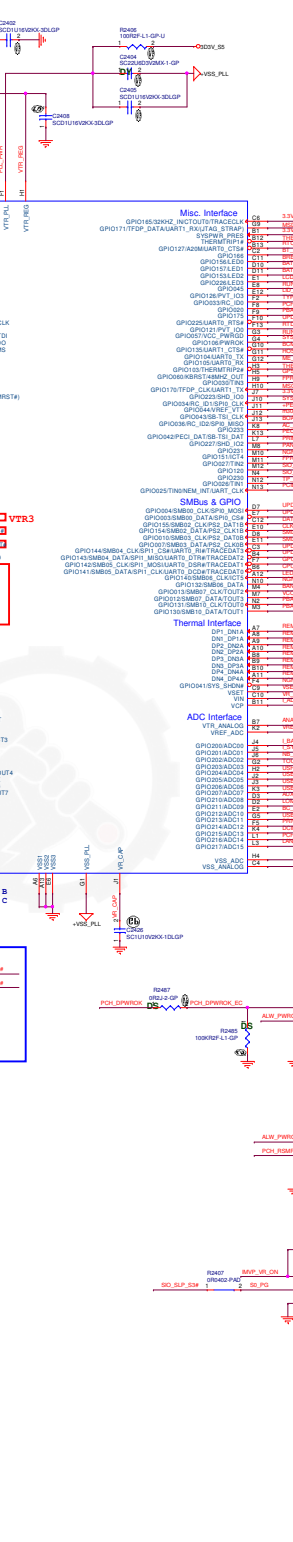
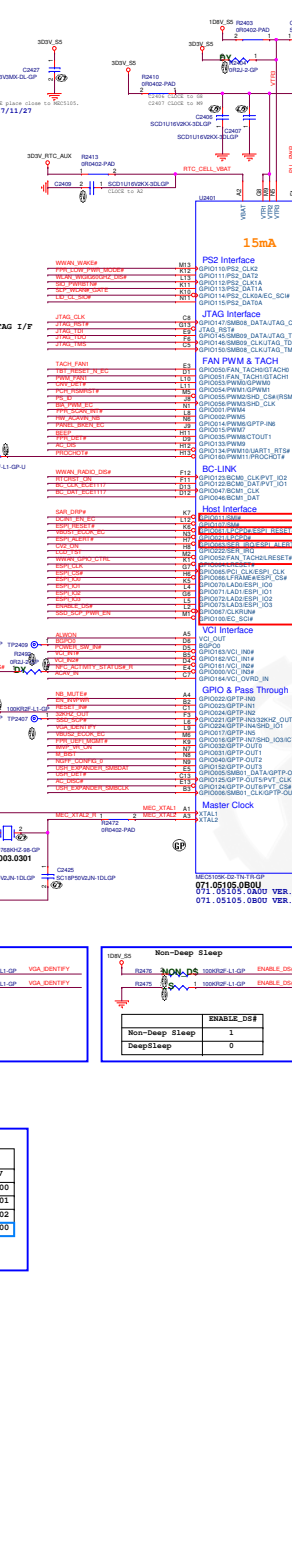
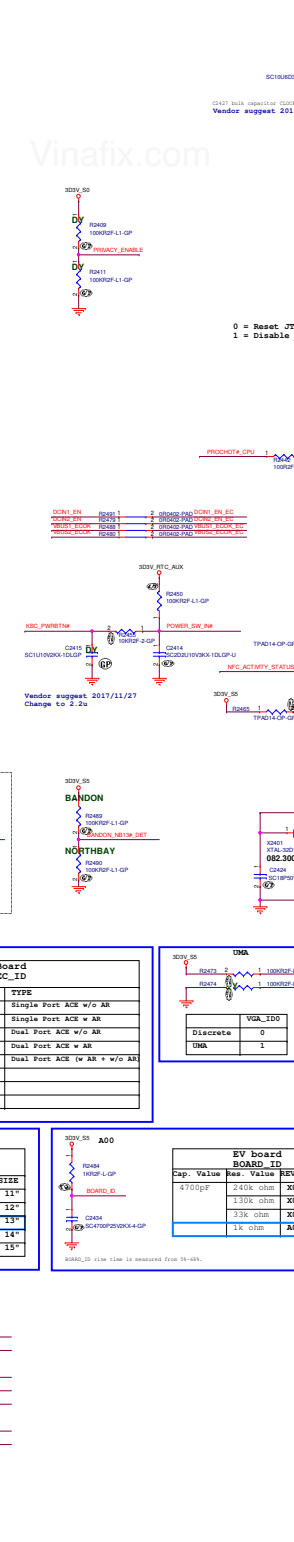
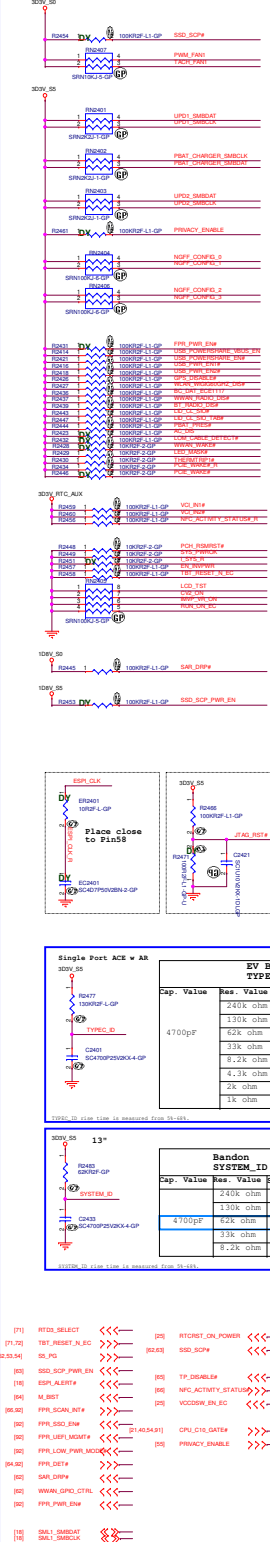
Bandon / NorthBay 13"

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Main Func = EC

- [10] SERIAL_MASTER
- [11] SERIAL_SLAVE
- [12] SERIAL_SLAVE
- [13] SERIAL_SLAVE
- [14] SERIAL_SLAVE
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- [98] SERIAL_SLAVE
- [99] SERIAL_SLAVE



Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
	52k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w/o AR
	8.2k ohm	Dual Port ACE w/o AR
	4.3k ohm	Dual Port ACE w/o AR
	2k ohm	Dual Port ACE w/o AR
	1k ohm	Dual Port ACE w/o AR

Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
	52k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w/o AR
	8.2k ohm	Dual Port ACE w/o AR
	4.3k ohm	Dual Port ACE w/o AR
	2k ohm	Dual Port ACE w/o AR
	1k ohm	Dual Port ACE w/o AR

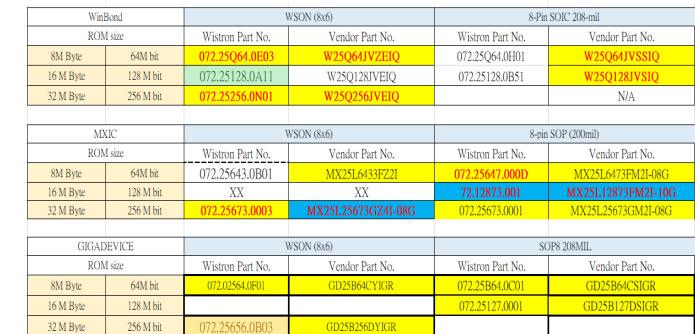
Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
	52k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w/o AR
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	4.3k ohm	Dual Port ACE w/o AR
	2k ohm	Dual Port ACE w/o AR
	1k ohm	Dual Port ACE w/o AR

Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
	52k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w/o AR
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	4.3k ohm	Dual Port ACE w/o AR
	2k ohm	Dual Port ACE w/o AR
	1k ohm	Dual Port ACE w/o AR

Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
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	33k ohm	Dual Port ACE w/o AR
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	2k ohm	Dual Port ACE w/o AR
	1k ohm	Dual Port ACE w/o AR

Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w/o AR
	52k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w/o AR
	8.2k ohm	Dual Port ACE w/o AR
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	1k ohm	Dual Port ACE w/o AR

SYSTEM SPI ROM

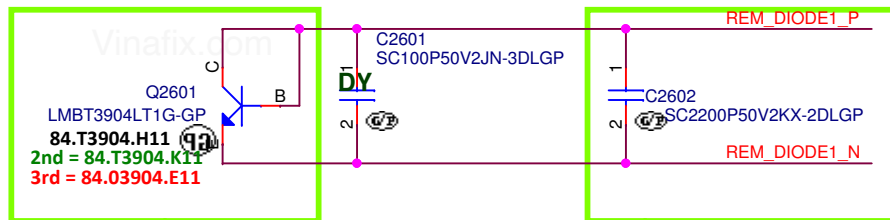


Title				Flash/RTC			
Size	A3	Document Number	Bandon / NorthBay 13"				Rev
Date:	Friday, February 15, 2019		Sheet	25	of	106	X00

Main Func = Thermal / FAN

[24] REM_DIODE1_P
[24] REM_DIODE1_N
[24] REM_DIODE2_P
[24] REM_DIODE2_N

[24] REM_DIODE4_P
[24] REM_DIODE4_N
[24] PWM_FAN1
[24] TACH_FAN1

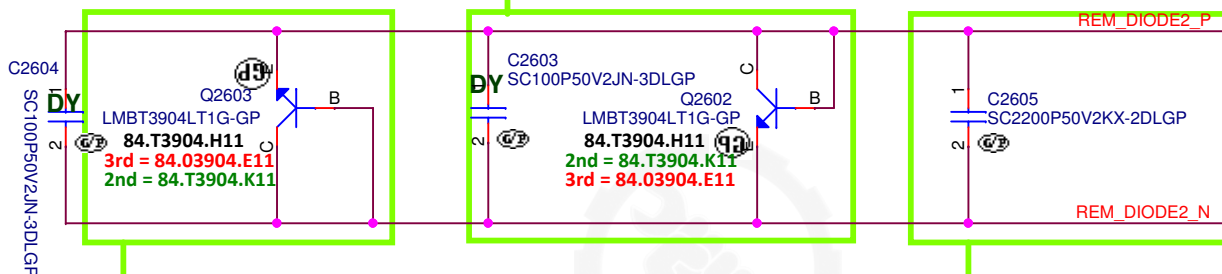


Layout Note: Place to CPU

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

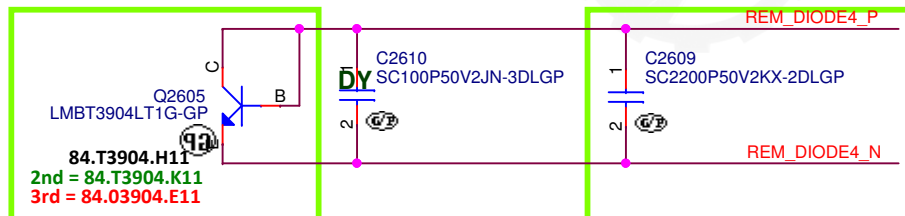
Layout Note: Close to WWAN/2nd SSD



Layout Note: Place to DIMM

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

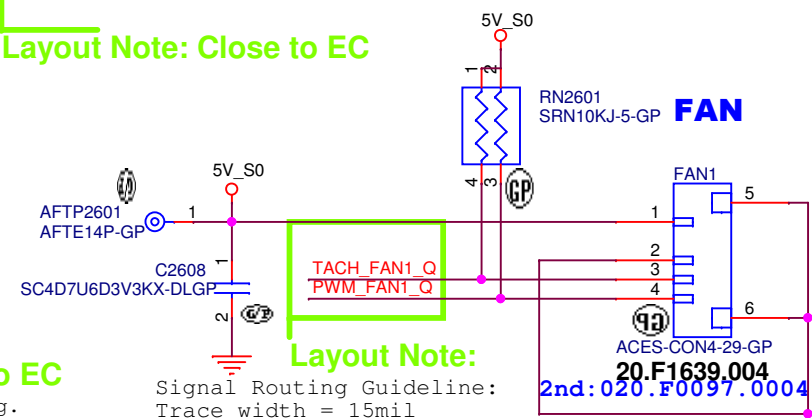
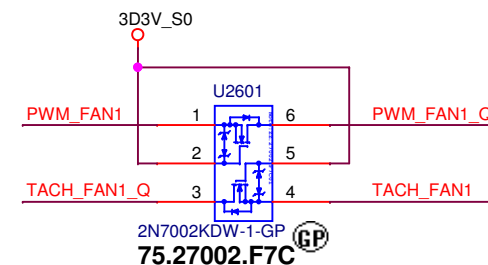


Layout Note: Place to V.R

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)



Layout Note:

Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q 1
PWM_FAN1_Q 1

<Core Design>



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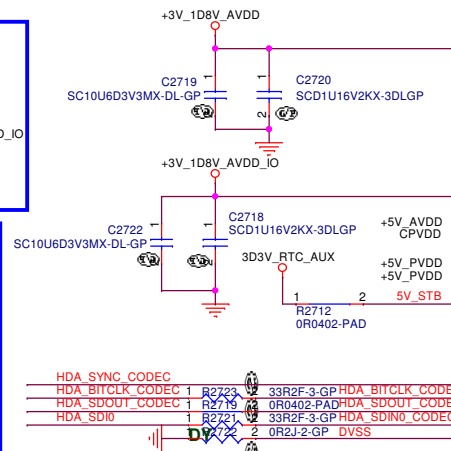
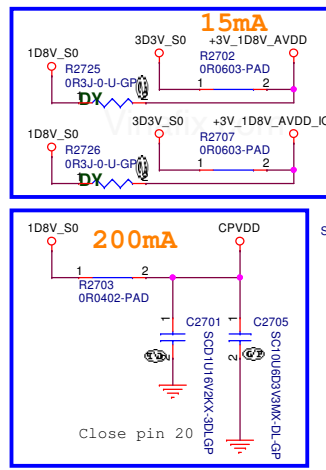
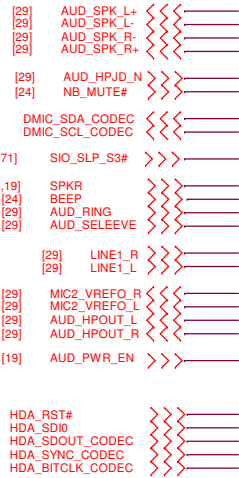
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title INT IO (Thermal/Fan)

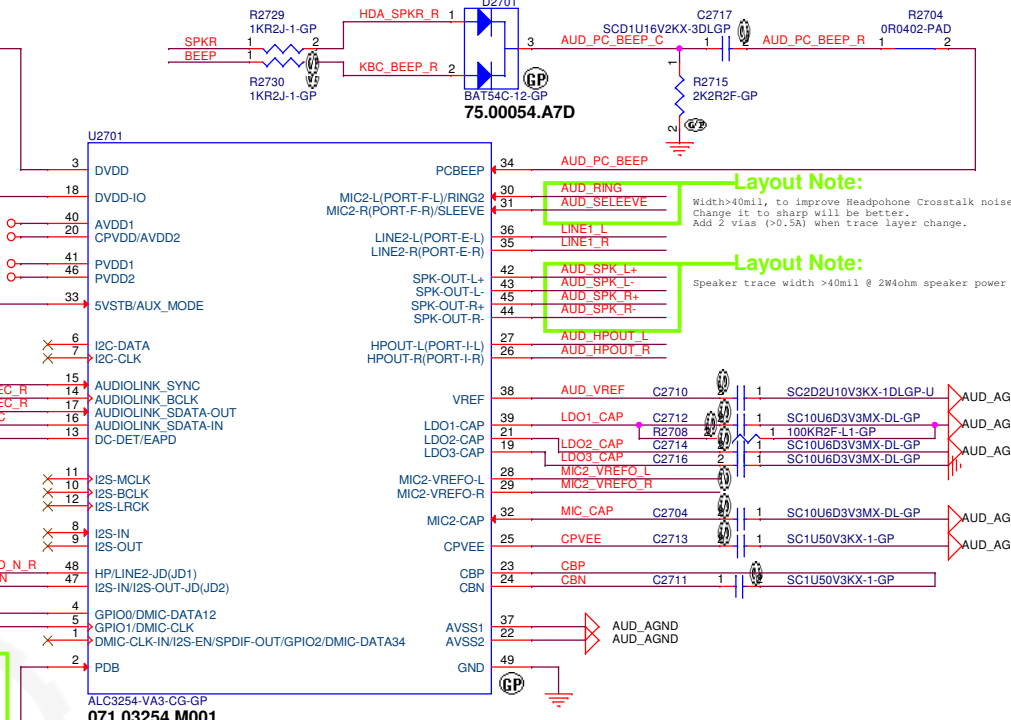
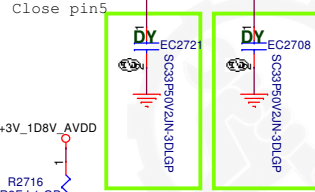
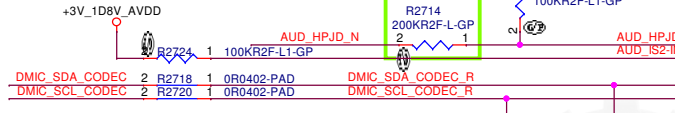
Size A4 Document Number Bandon / NorthBay 13" Rev X00

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Main Func = Audio

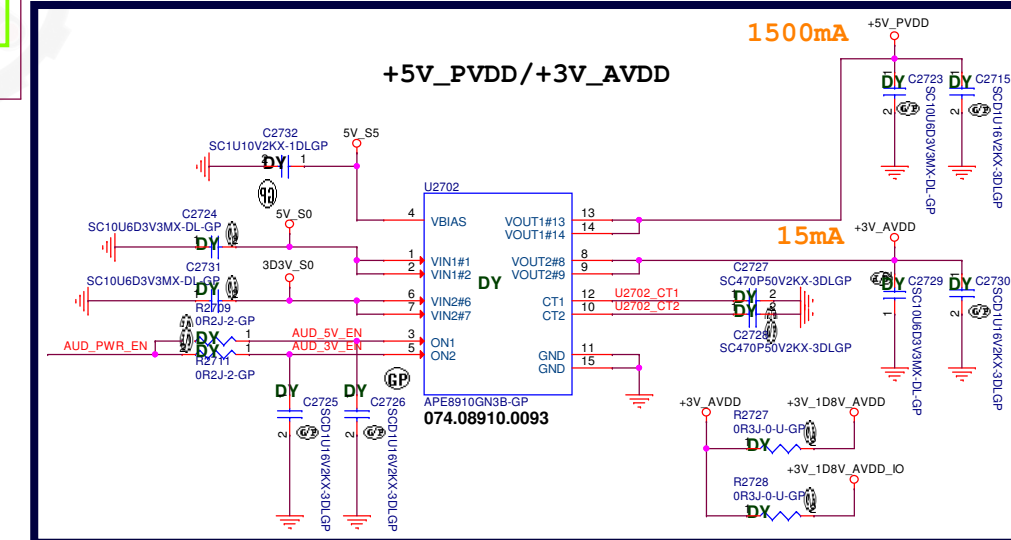
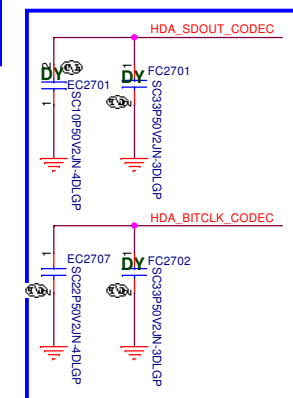
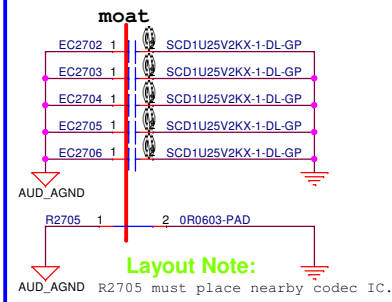
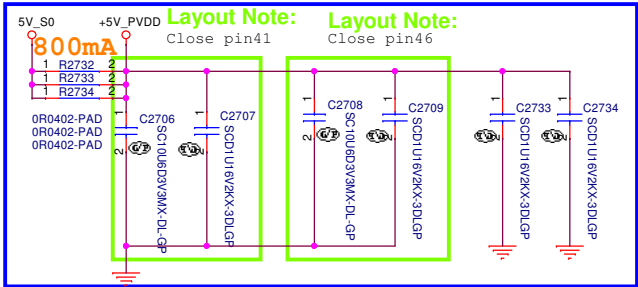
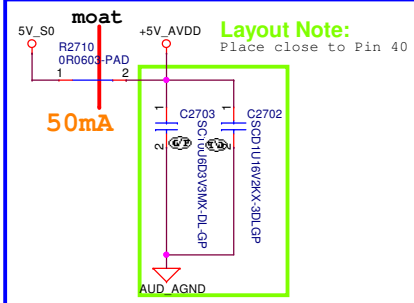


Layout Note:
Place close to Pin 1



Layout Note:
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



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Audio (CodecALC3253)

Size A3 Document Number **Bandon / NorthBay 13"** Rev **X00**


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EMI suggest change to 33p
2015/12/02
Azalia I/F EMI

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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Audio (RSVD) (Audio AMP)					
Size	Document Number				Rev
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
Date: Friday, February 15, 2019		Sheet 30 of	106

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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
LAN (RSVD) (Giga_RTL8151GD)					
Size		Document Number			Rev
A4		Bandon / NorthBay 13"			X00
Date:		Friday, February 15, 2019		Sheet	31 of 106

Main Func = LAN

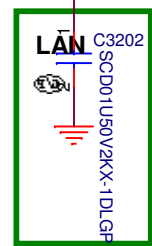
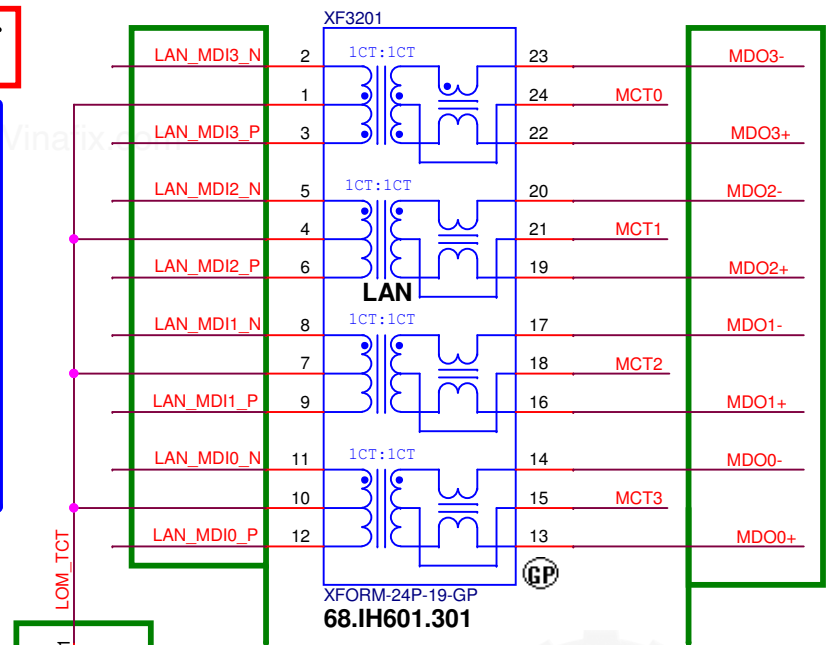
[24,64] LED_MASK#
[97] LAN_0_GREEN_LINK_N
[97] LAN_1_AMBER_ACT_N

[97] LAN_MDI0_P
[97] LAN_MDI0_N

[97] LAN_MDI1_P
[97] LAN_MDI1_N

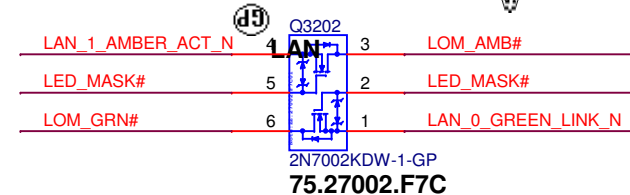
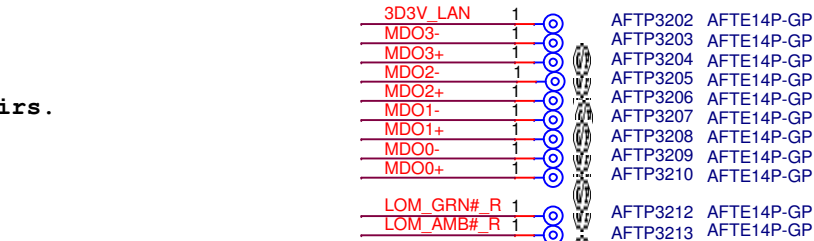
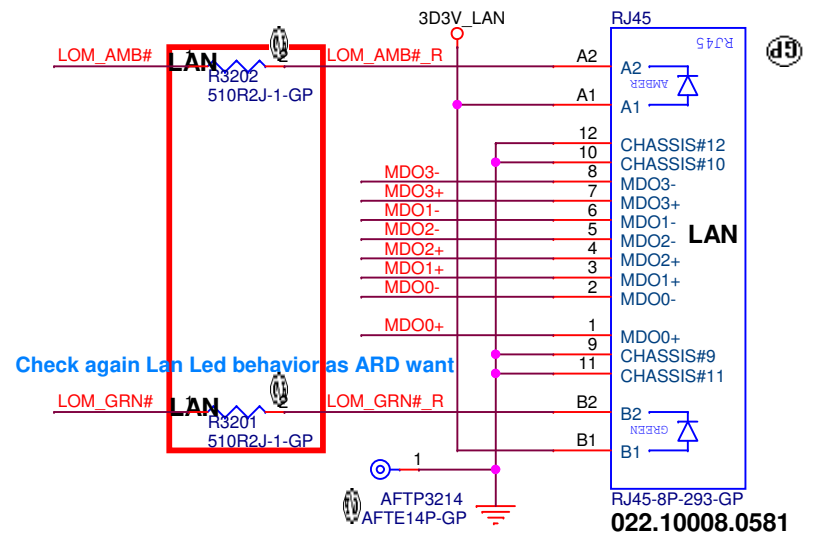
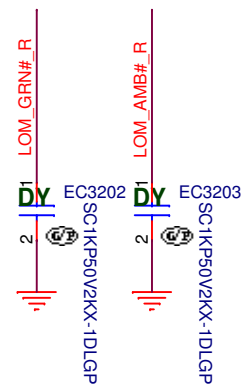
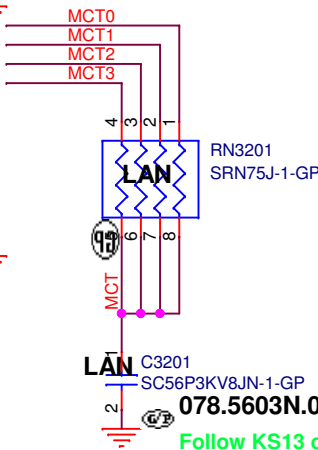
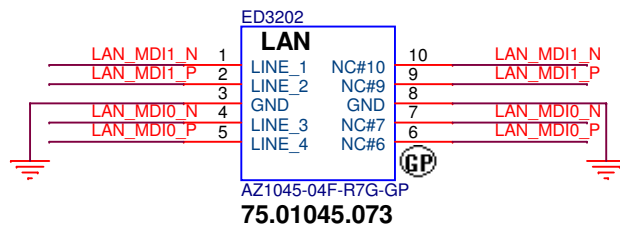
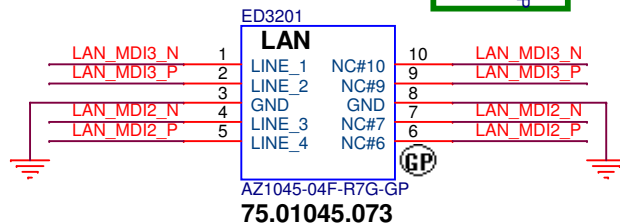
[97] LAN_MDI2_P
[97] LAN_MDI2_N

[97] LAN_MDI3_P
[97] LAN_MDI3_N



Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

<Core Design>



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Title **LAN (RJ45+Transformer)**

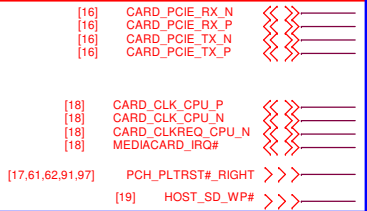
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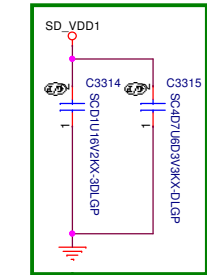
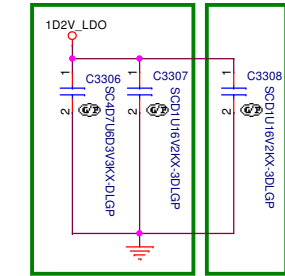
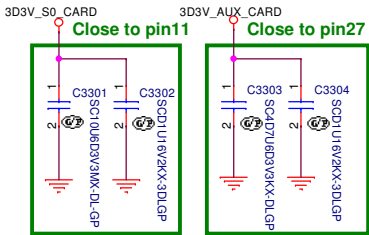
Main Func = Card Reader

3D3V_S0_CARD

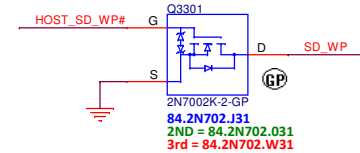
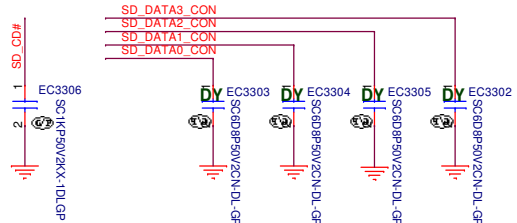
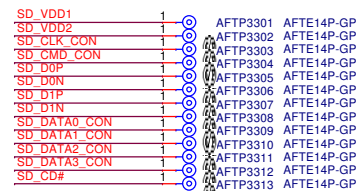
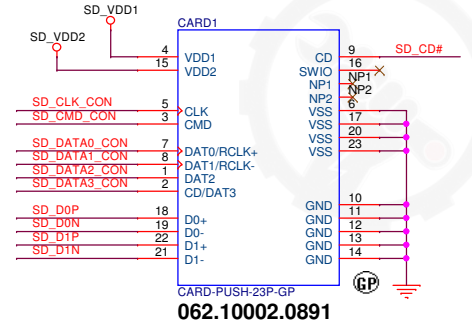
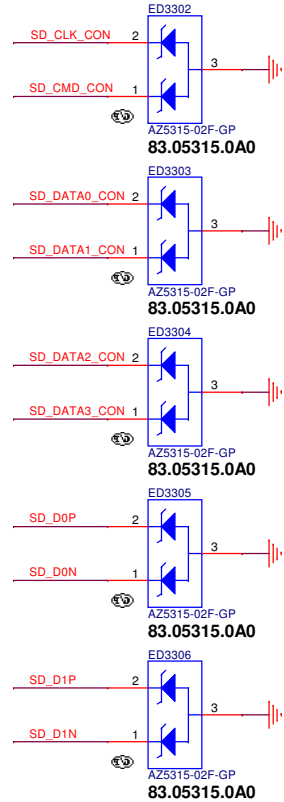
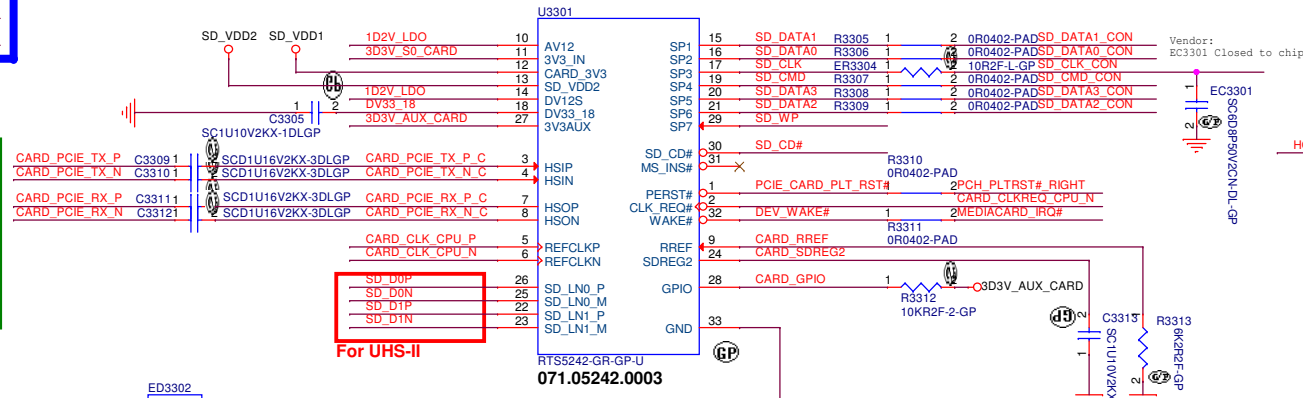
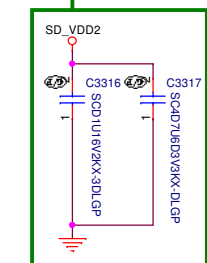
850mA



Layout Note:



Layout Note:Close to Card Reader CONN



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Title **CARDREADER (SDIO/SD Conn)**


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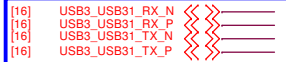
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD) (USB2.0 CONN)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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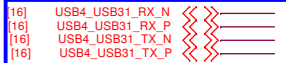
Main Func = USB 3.0

USB4/USB30-3/USB20-3/PowerShare

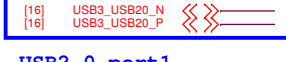
USB3.1 PORT1



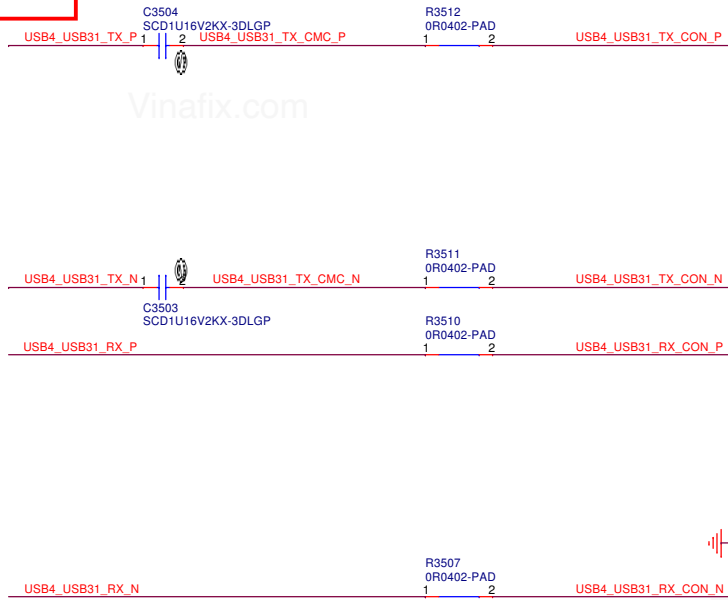
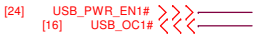
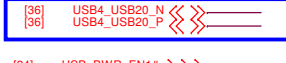
USB3.1 PORT2



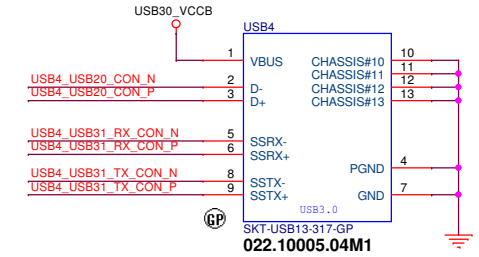
USB2.0 port2



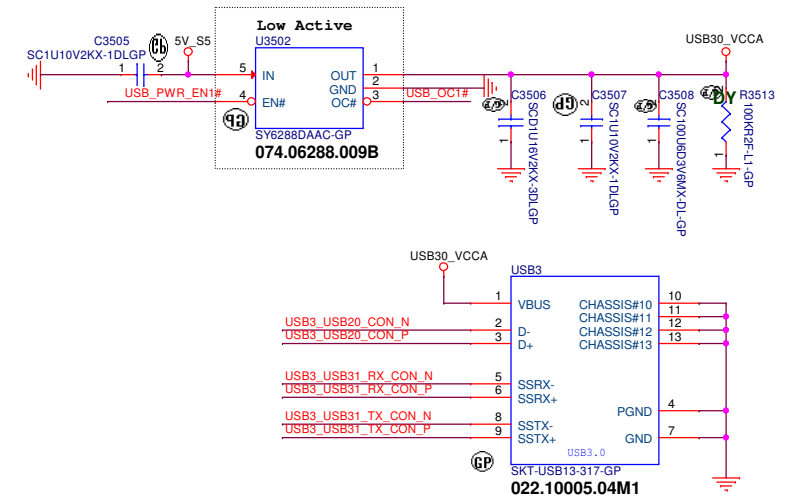
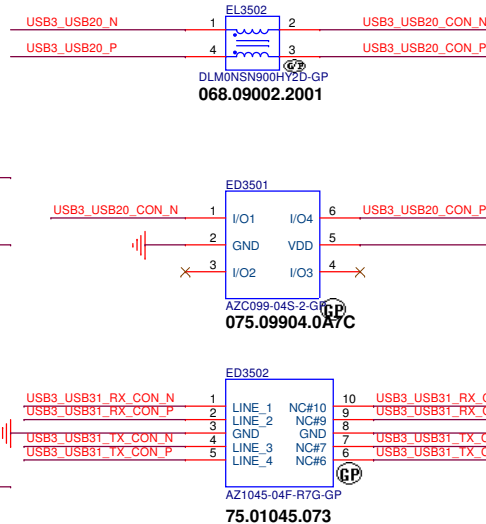
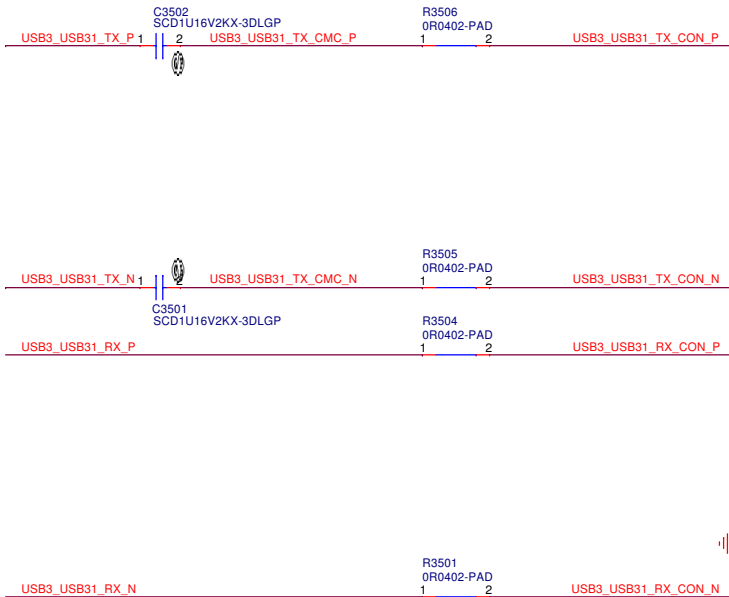
USB2.0 port1



EXT Port1 Right Side, Support Power Share



USB3/USB30-3/USB20-2





<Core Design>

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Title		USB (USB3.0 Conn)	
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support power share on the USB3.0 port on the right side of platform


USB2.0 port2


[35] USB4_USB20_N   _____
[35] USB4_USB20_P _____

[24] USB_POWERSHARE_VBUS_EN >>> _____
[24] USB_POWERSHARE_EN# >>> _____

[16] USB_OC0# <<<_____

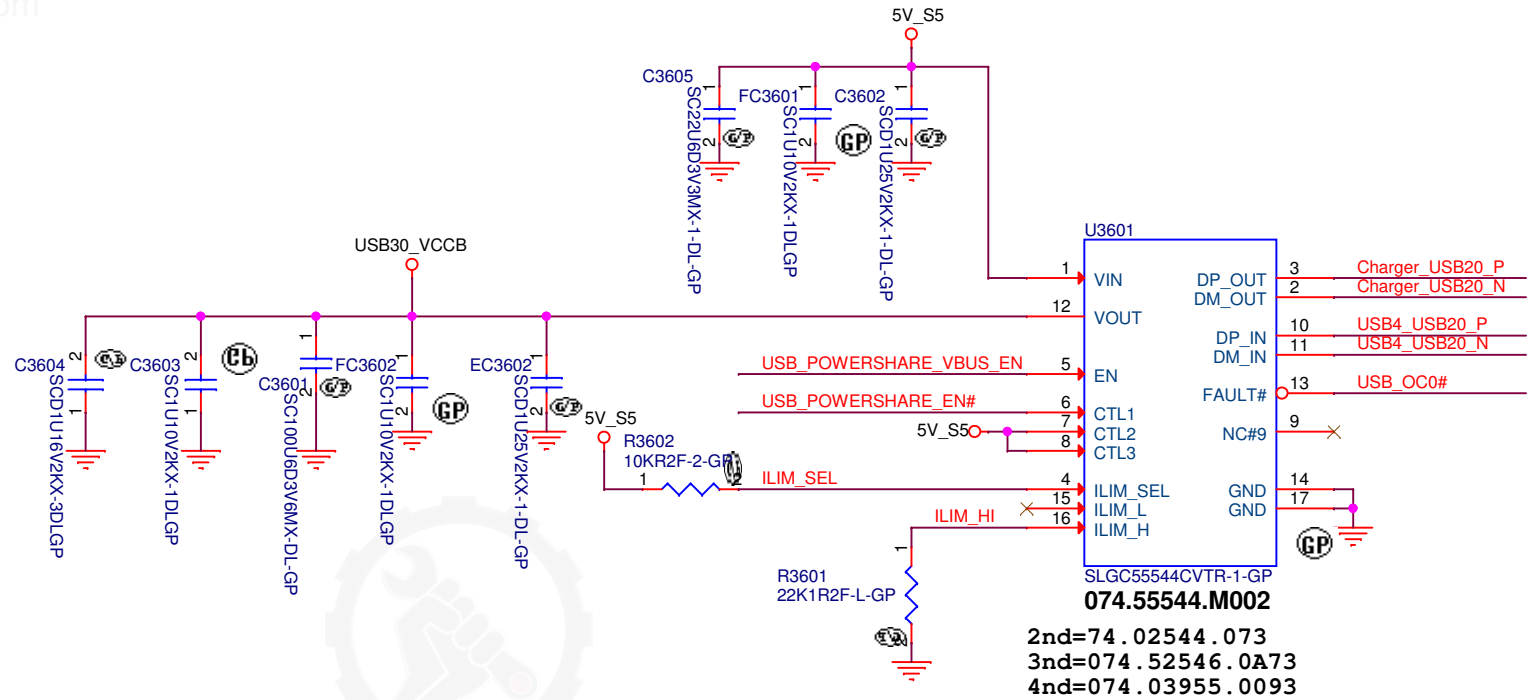
USB charger

[16] Charger_USB20_N  _____

[16] Charger_USB20_P  _____

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570



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Title

USB (USB Charger)

Size
A4

Document Number

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Rev
X00


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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <i>USB (RSVD) (PCIE to USB3.0)</i>		
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5

4

3


2

1

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<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD)(USB3.0 Redriver)		
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Date: Friday, February 15, 2019		Sheet 38 of 106

Main Func =

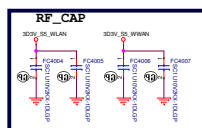
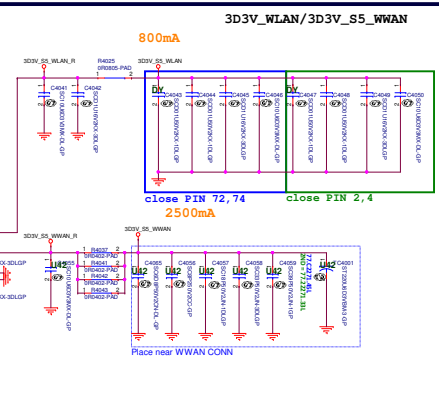
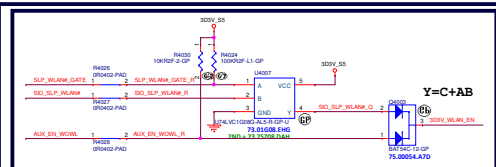
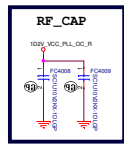
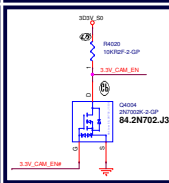
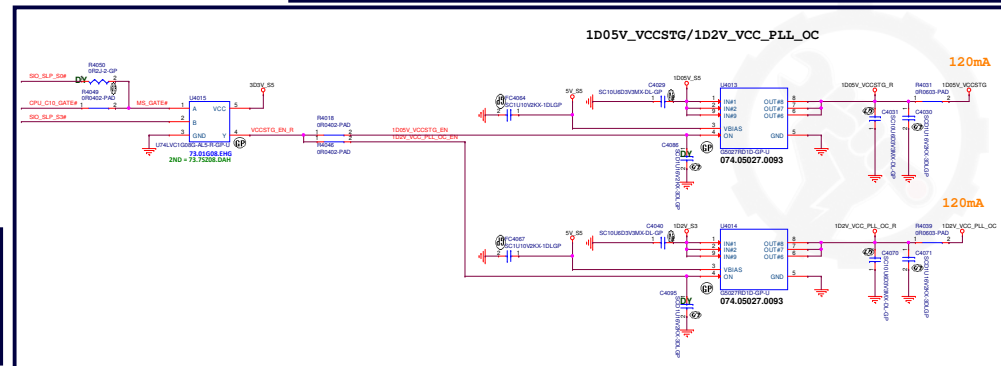
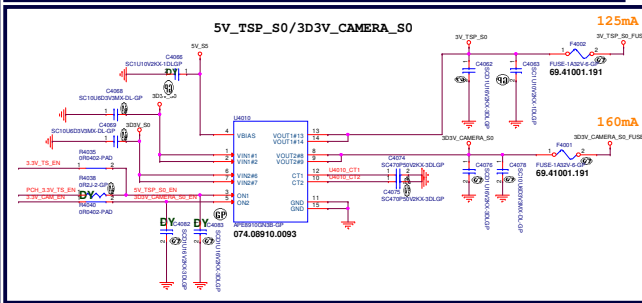
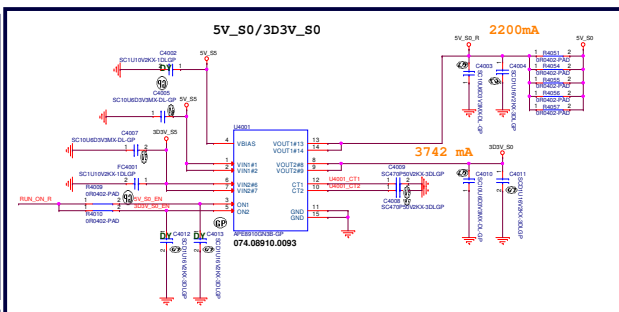
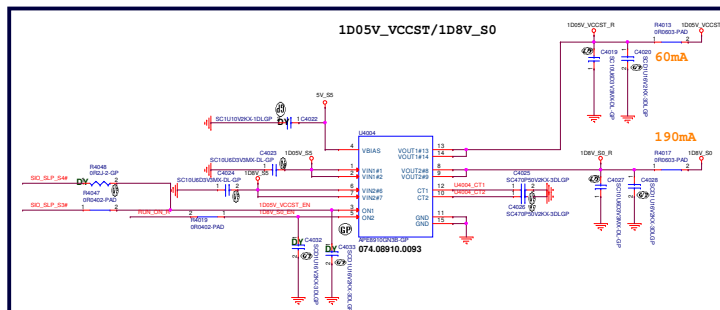
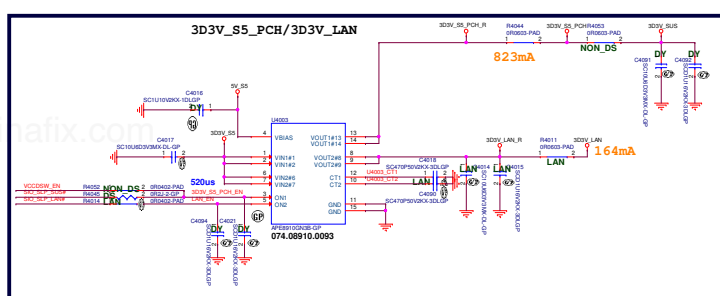
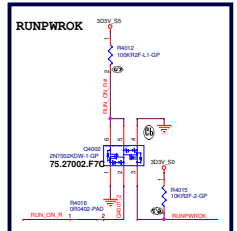
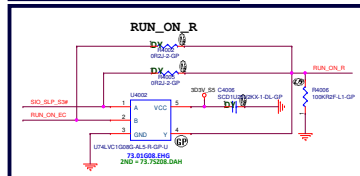
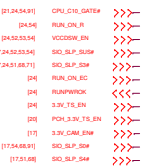
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence (RSVD)			
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[24]	ALWON	>>>—
[45]	3V5V_EN	<<<—
[45]	303V_PG	>>>—
[45]	5V_PG	>>>—
	ALW_PWRIGD_3V_5V	<<<—
[17]	SIO_SLP_LAN#	>>>—
[24]	SLP_WLAN#_GATE	>>>—
[17]	SIO_SLP_WLAN#	>>>—
	AUX_EN_WOW#	>>>—
[24]	3.5V_WWAN_EN	>>>—



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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Sequence (RSVD) (DS3/S0ix)		
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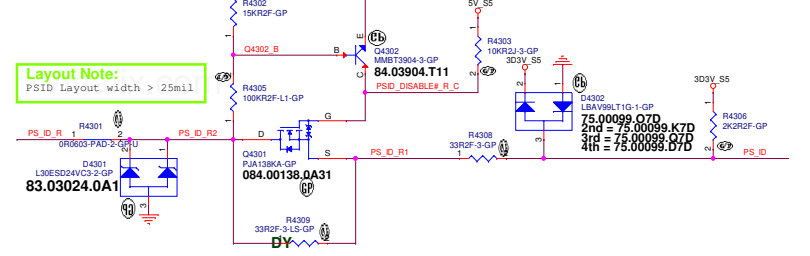
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)			
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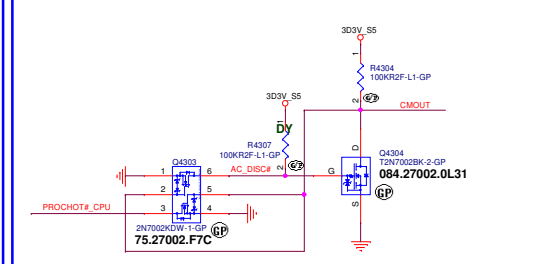
Main Func = DCIN & BATT Com

[24] PS_ID <<< ---
[3,24,44,4] PROCHOT#_CPU <<< ---
[44] CMOUT <<< ---
[24,44] AC_DIS >>> ---
[24] DCN2_EN >>> ---
[24,44] PBAT_CHARGER_SMBCLK <<< ---
[24,44] PBAT_CHARGER_SMBDAT <<< ---
[24,44] PBAT_CHARGER_SMBPES# <<< ---
[24,44] PBAT_CHARGER_SMBPES# <<< ---
[74] PWR_VBUS_OVP_OUT_R >>> ---
[24,44] AC_DISC# <<< ---
[24,44,74] HW_ACAVIN_NB <<< ---
[24,74] VBUS1_ECOK >>> ---

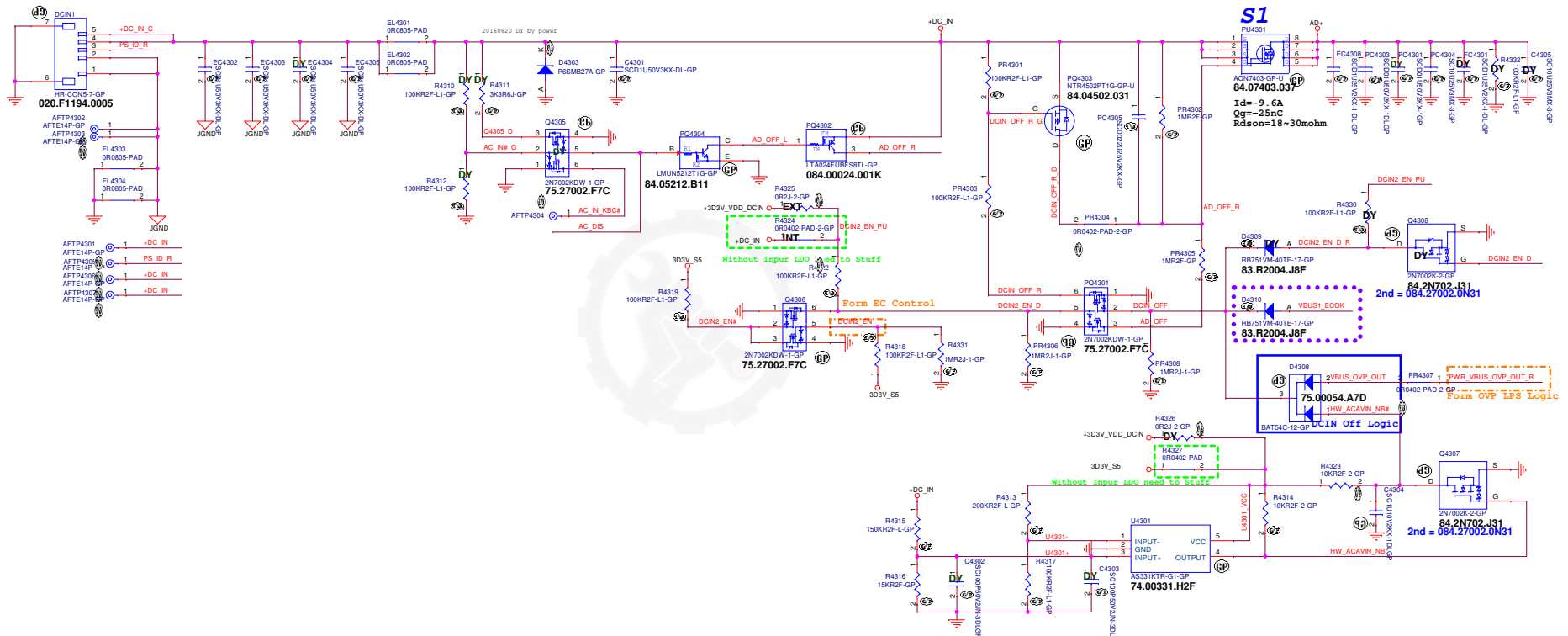
PSID



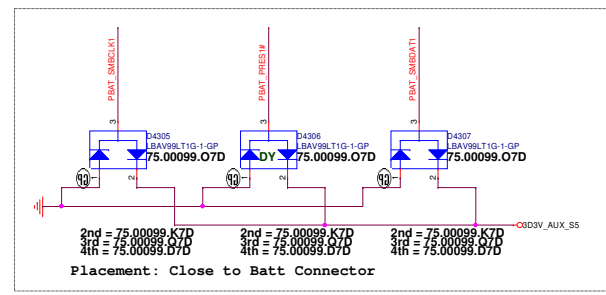
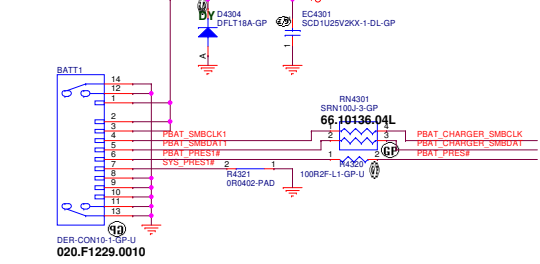
AC Disconnect Latch



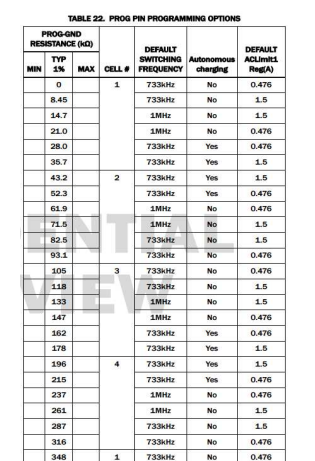
DC_IN



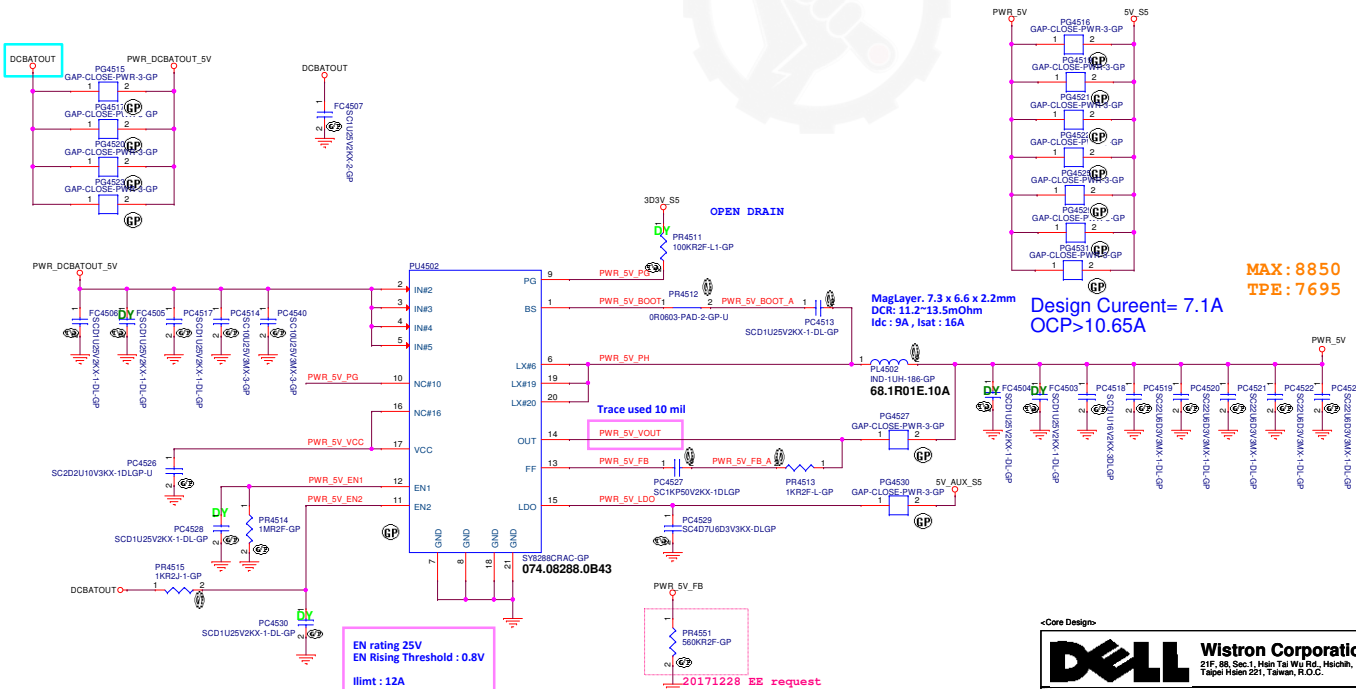
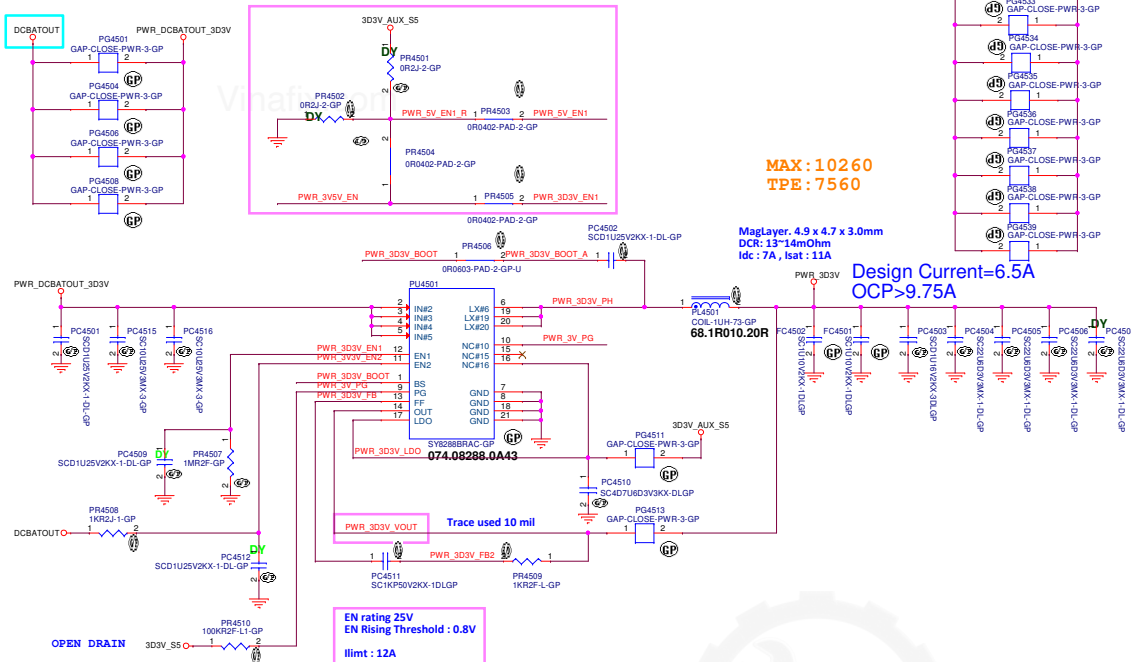
Batt Connector



```
Main Func = Power_Charger
```

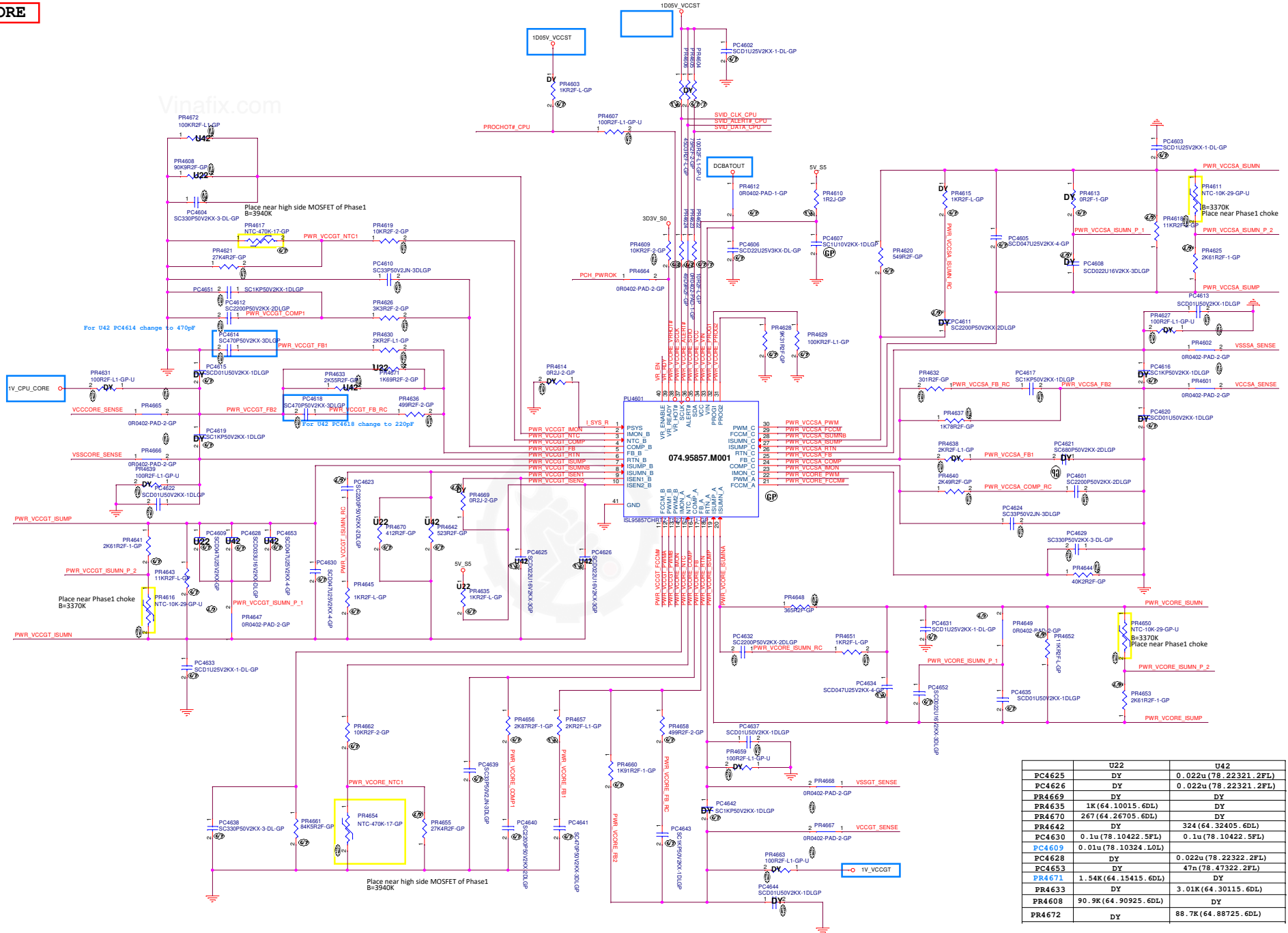


Main Func = Power_System 5V/3D3V



Main Func = CPU_CORE

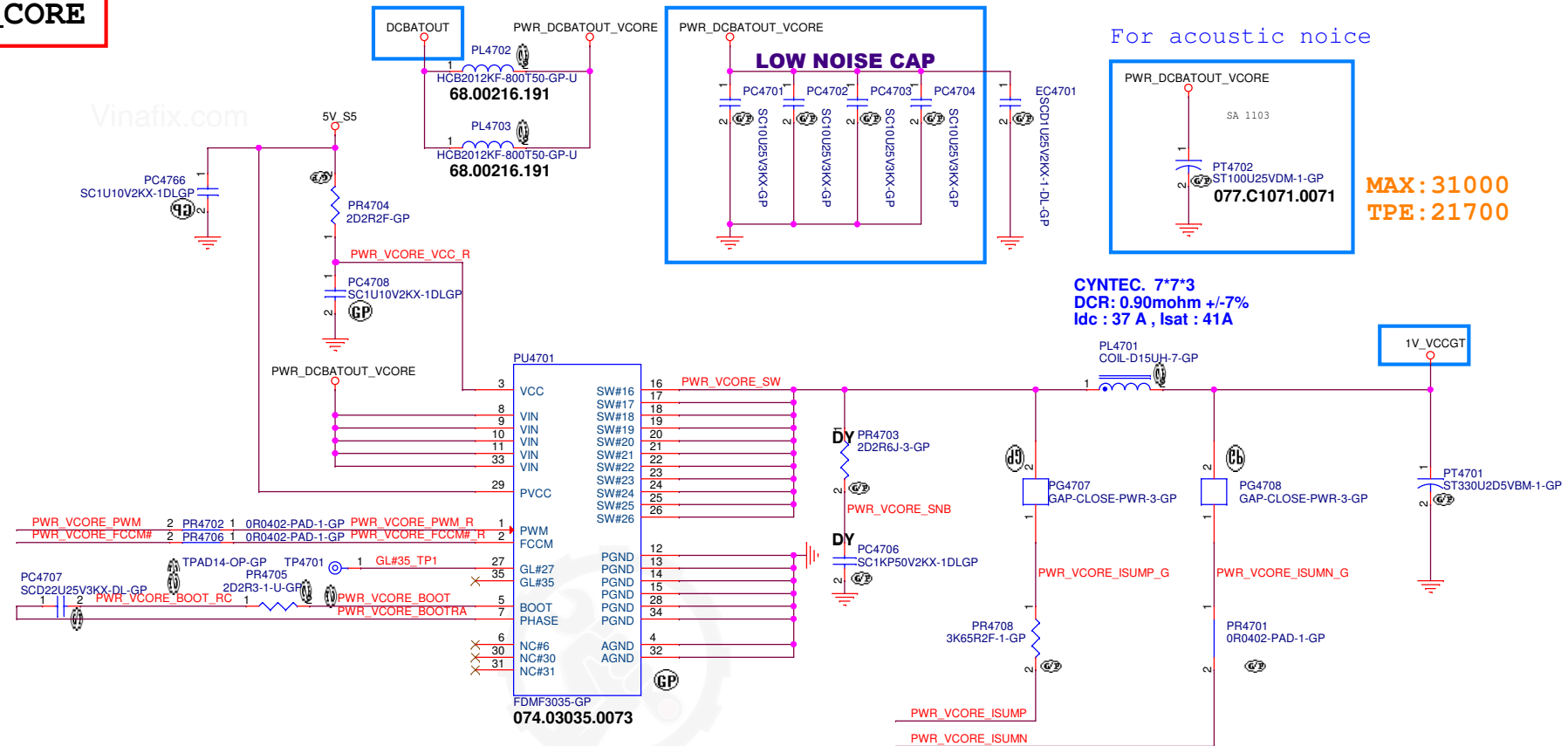
- [7] SVD_CLK_CPU <<<
- [7] SVD_ALERT#_CPU <<<
- [7] SVD_DATA_CPU <<<
- [7] VCCORE_SENSE <<<
- [7] VSSCORE_SENSE <<<
- [48] PWR_VCCGT_ISUMP >>>
- [48] PWR_VCCGT_ISUMN >>>
- [48] PWR_VCCGT_ISEN1 >>>
- [48] PWR_VCCGT_ISEN2 >>>
- [8] VSSGT_SENSE <<<
- [8] VCCGT_SENSE <<<
- [47] PWR_VCORE_ISUMN >>>
- [47] PWR_VCORE_ISUMP >>>
- [50] PWR_VCCSA_ISUMN >>>
- [50] PWR_VCCSA_ISUMP >>>
- [8] VSSSA_SENSE <<<
- [8] VCCSA_SENSE <<<
- [48] PWR_VCCGT_FCCM >>>
- [48] PWR_VCCGT_PWM >>>
- [50] PWR_VCCSA_PWM >>>
- [50] PWR_VCCSA_FCCM >>>
- [47] PWR_VCORE_PWM >>>
- [47] PWR_VCORE_FCCM >>>
- [24] VR_EN >>>
- [3,24,43,44] PROCHOT#_CPU <<<
- [17] PCH_PWROK <<<
- [24,44] LSYS_R <<<



	U22	U42
PC4625	DY	0.022u (78.22321.2FL)
PC4626	DY	0.022u (78.22321.2FL)
PR4669	DY	DY
PR4635	1K (64.10015.6DL)	DY
PR4670	267 (64.26705.6DL)	DY
PR4642	DY	324 (64.32405.6DL)
PC4630	0.1u (78.10422.5FL)	0.1u (78.10422.5FL)
PC4609	0.01u (78.10324.10L)	
PC4628	DY	0.022u (78.22322.2FL)
PC4653	DY	47n (78.47322.2FL)
PR4671	1.54K (64.15415.6DL)	DY
PR4633	DY	3.01K (64.30115.6DL)
PR4608	90.9K (64.90925.6DL)	DY
PR4672	DY	88.7K (64.88725.6DL)

Main Func = CPU_CORE

[46] PWR_VCORE_PWM >>>
[46] PWR_VCORE_FCCM# >>>
[46] PWR_VCORE_ISUMP <<<
[46] PWR_VCORE_ISUMN <<<



<Core Design>



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Title			ISL95859C_CPU_VCORE(2/3)
Size	Document Number	Rev	X00
Custom	Bandon / NorthBay 13"		
Date:	Friday, February 15, 2019	Sheet	47 of 106

[46]	PWR_VCCGT_PWMA	»
[46]	PWR_VCCGT_FCCM#	»
[46]	PWR_VCCGT_ISEN1	«
[46]	PWR_VCCGT_ISUMP	«
[46]	PWR_VCCGT_ISUMN	«
[46]	PWR_VCCGT_ISEN2	«
[46]	PWR_VCCGT_PWMB	»




Size Custom	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019	Sheet 48 of	106

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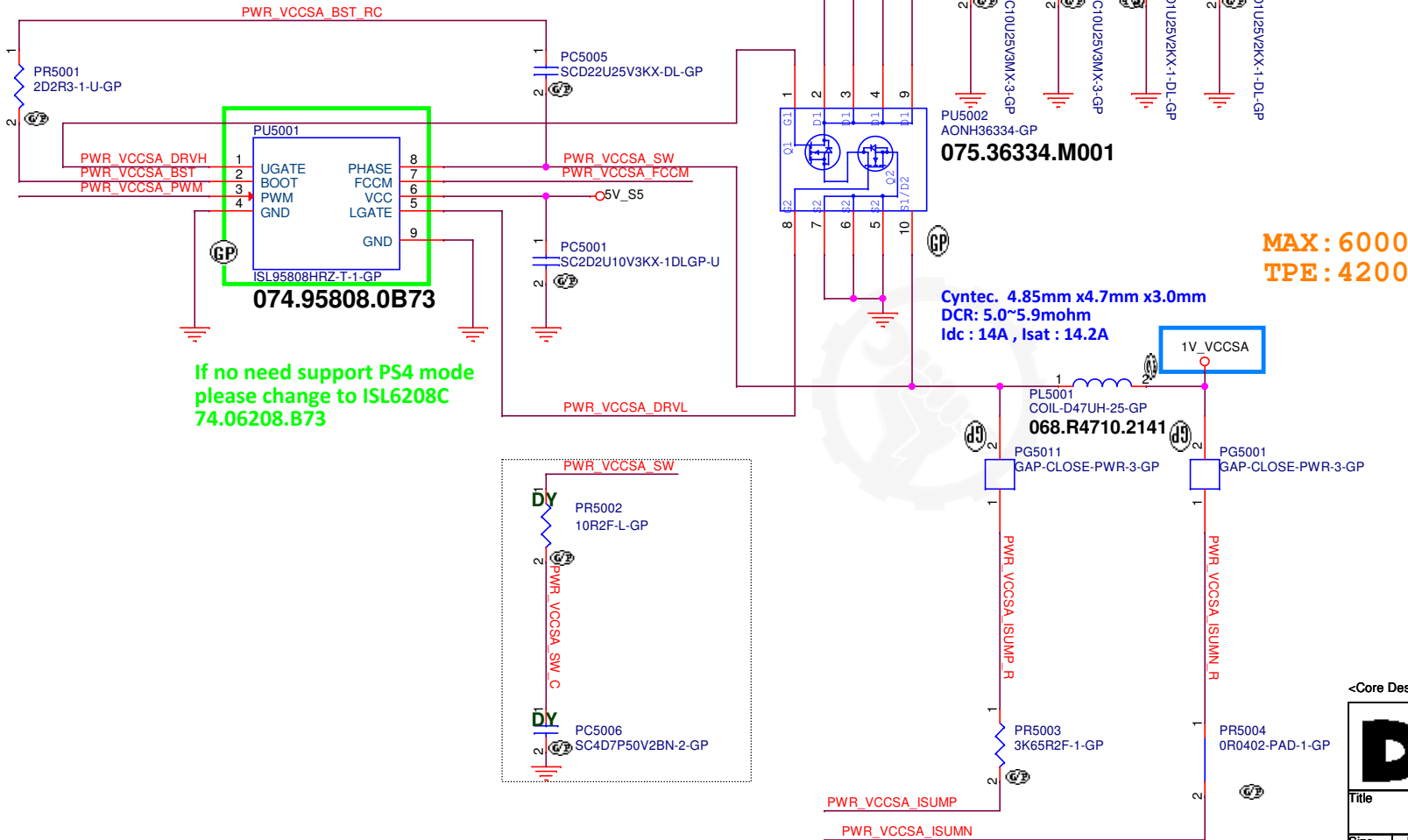
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title NCP81210MN_CPU_VCCGTUS					
Size A4		Document Number Bandon / NorthBay 13"			Rev X00
Date: Friday, February 15, 2019		Sheet 49		of 106	

Main Func = CPU_VCCSA

[46] PWR_VCCSA_PWM >>>—
[46] PWR_VCCSA_ISUMP <<<—
[46] PWR_VCCSA_ISUMN <<<—
[46] PWR_VCCSA_FCCM >>>—

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<Core Design>



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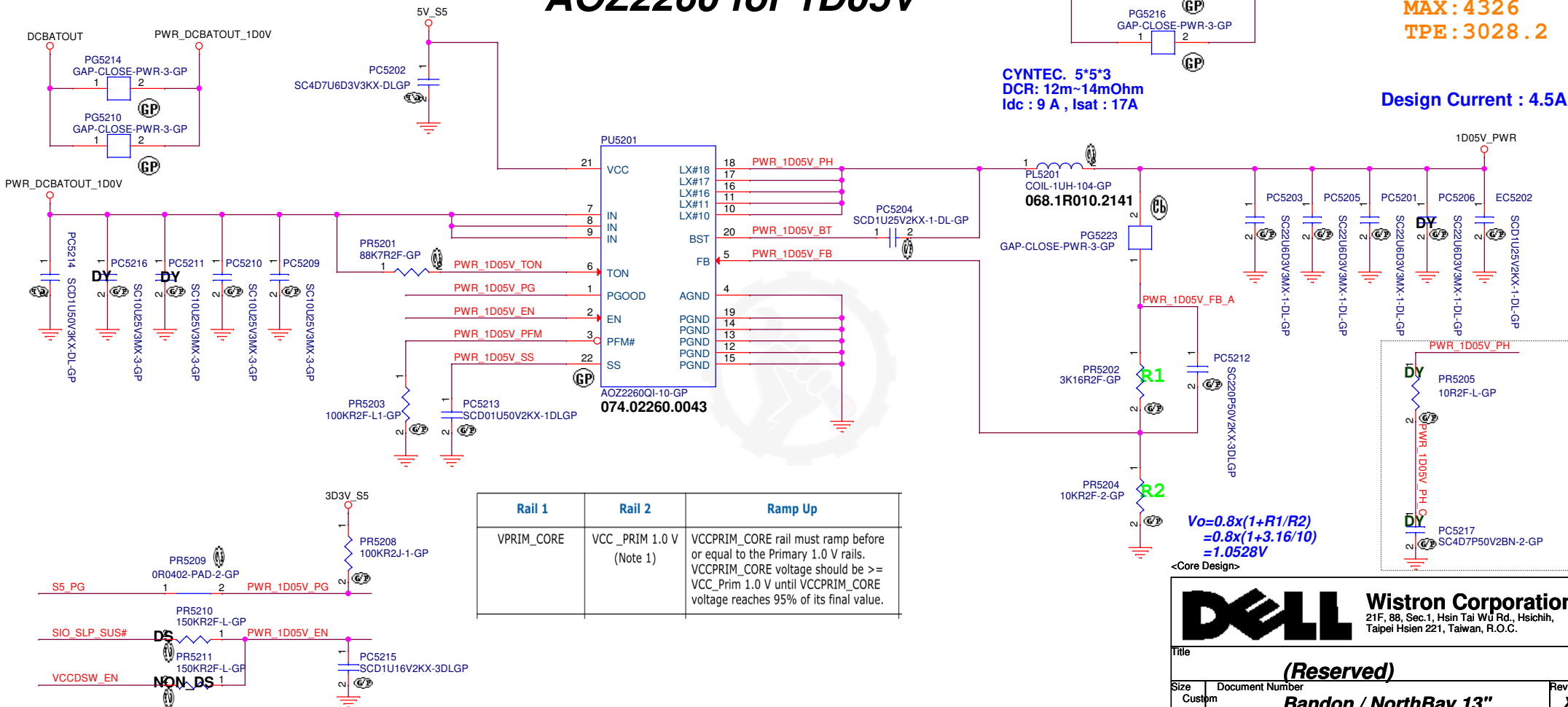
Title		VCCSA	
Size	Document Number	Rev	
Custom	Bandon / NorthBay 13"	X00	
Date:	Friday, February 15, 2019	Sheet	50 of 106

SSID = PWR.Plane.Regulator_1D05V

[24,53,54] S5_PG <<<—
[17,24,40,53,54] SIO_SLP_SUS# >>>—
[24,40,53,54] VCCDSW_EN >>>—

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AOZ2260 for 1D05V



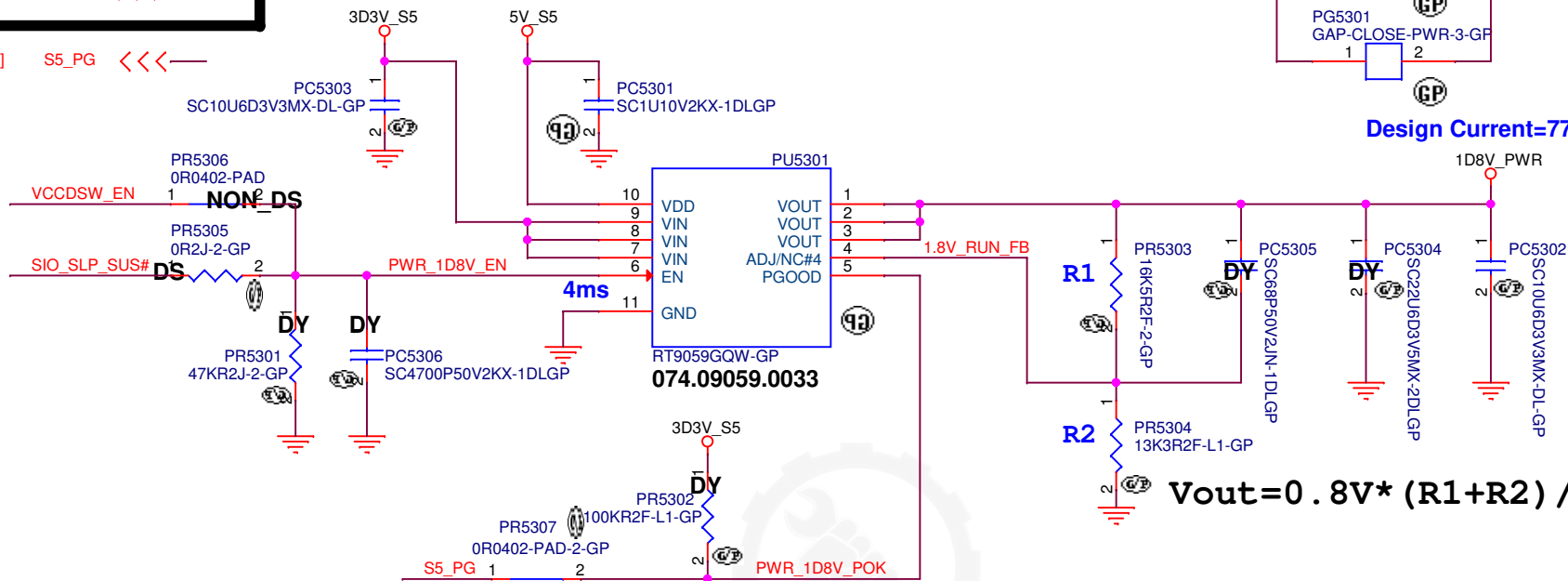
Main Func = 1D8V

APL5934 for 1D8V_S5

MAX: 917
TPE: 641.9

Design Current=770mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$



<Core Design>



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Title

(Reserved)

Size
A4

Document Number

Bandon / NorthBay 13"

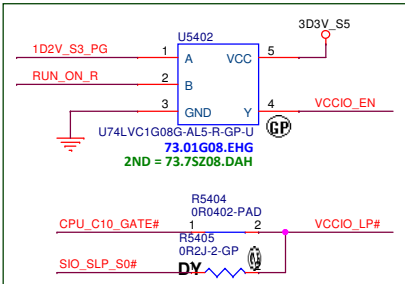
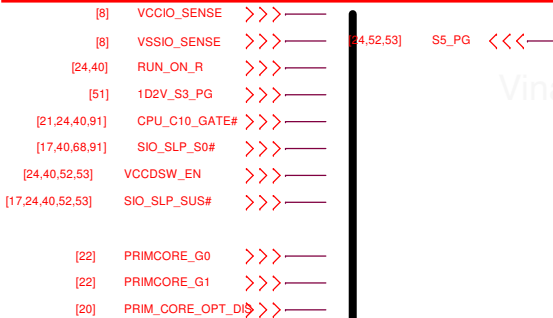
Rev

X00

Date: Friday, February 15, 2019

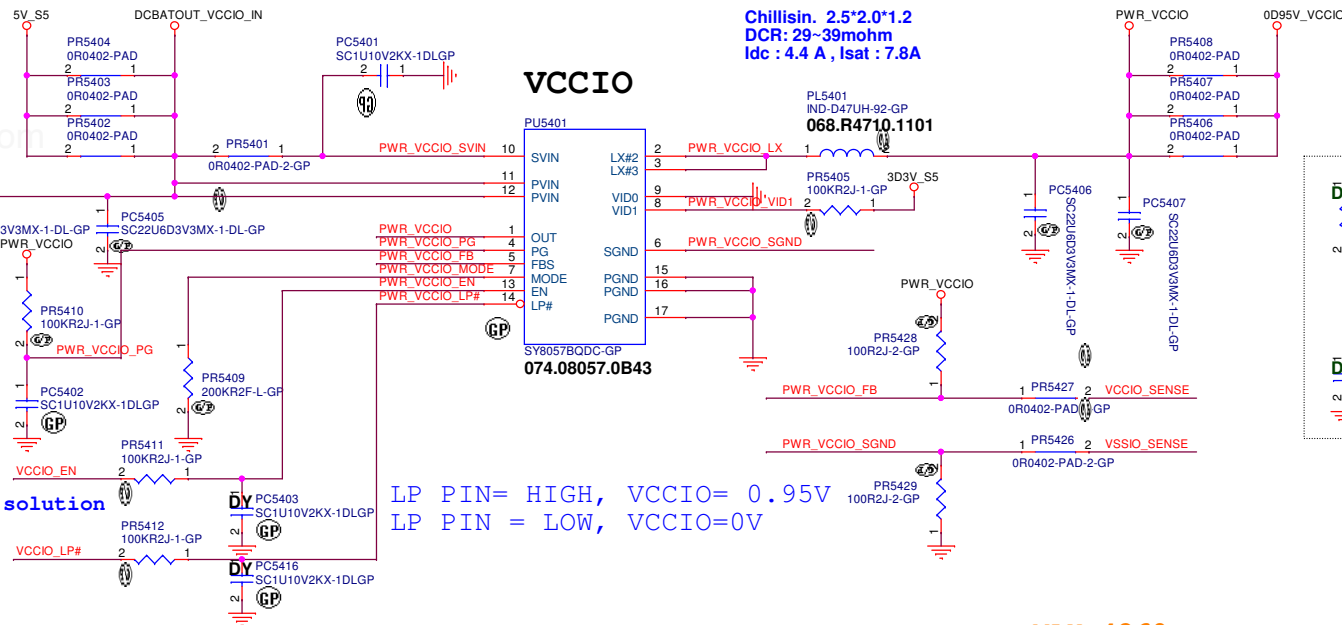
Sheet 53 of 106

Main Func = VCCIO / VCCPRIM



EV2 test use RC solution

LP PIN= HIGH, VCCIO= 0.95V
LP PIN = LOW, VCCIO=0V



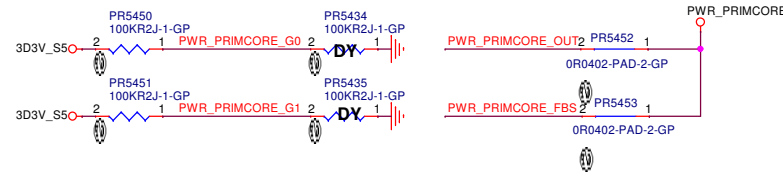
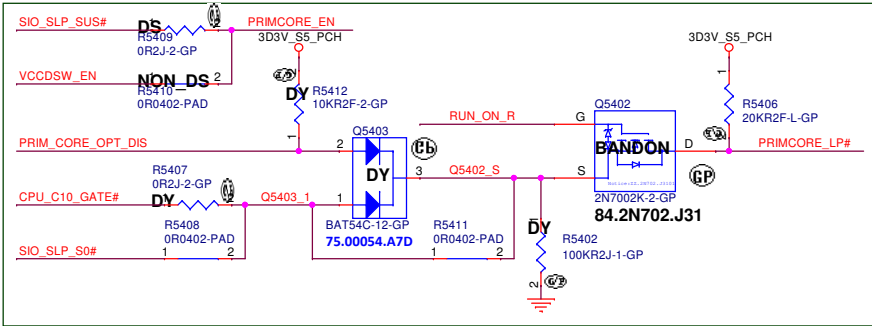
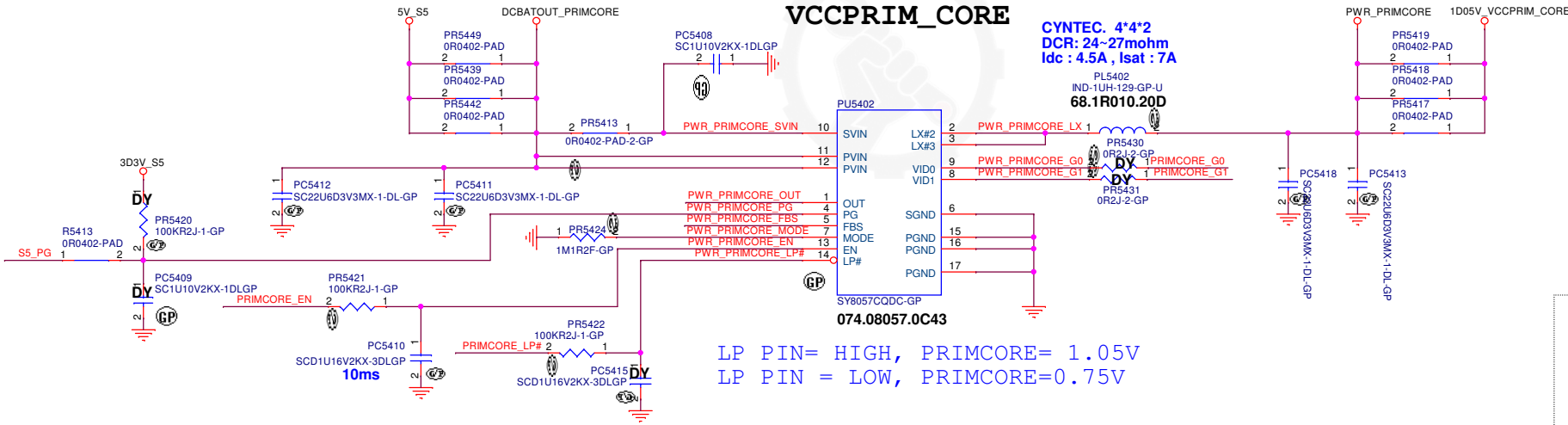
MAX: 1000
TPE: 700

MAX: 4260
TPE: 2982

VCCPRIM_CORE

CYNTEC. 4*4*2
DCR: 24~27mohm
Idc : 4.5A , Isat : 7A

LP PIN= HIGH, PRIMCORE= 1.05V
LP PIN = LOW, PRIMCORE=0.75V



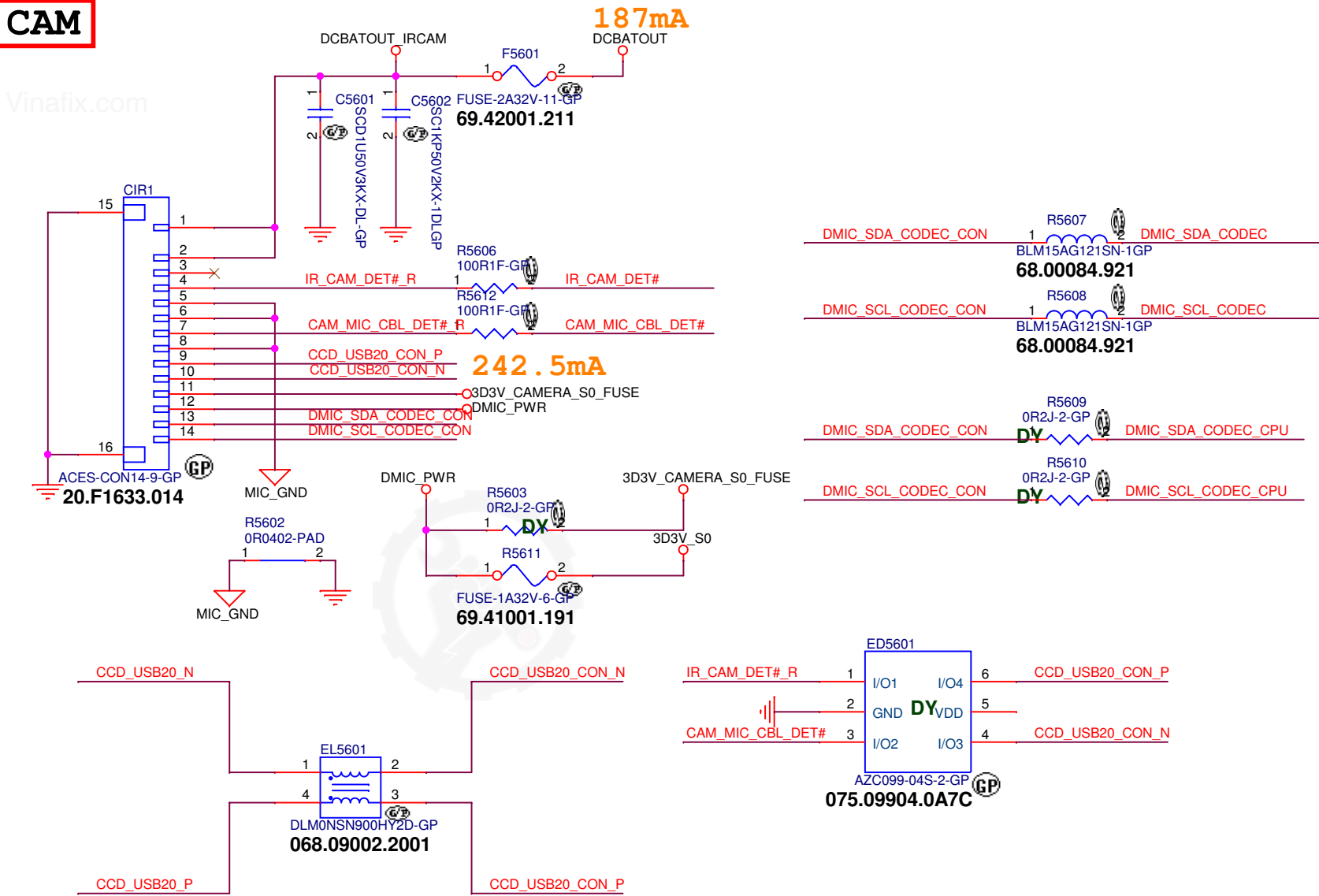
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Title	<Title>		
Size	A3	Document Number	Bandon / NorthBay 13"
Date:	Friday, February 15, 2019	Sheet	54 of 106
Rev	X00		


Main Func = IR CAM

CAMERA

[16]	CCD_USB20_N	<<<<
[16]	CCD_USB20_P	<<<<
[27]	DMIC_SDA_CODEC	>>>>
[27]	DMIC_SCL_CODEC	>>>>
[20]	IR_CAM_DET#	<<<<
[19]	CAM_MIC_CBL_DET#	<<<<
[19]	DMIC_SDA_CODEC_CPU	>>>>
[19]	DMIC_SCL_CODEC_CPU	>>>>



<Core Design>



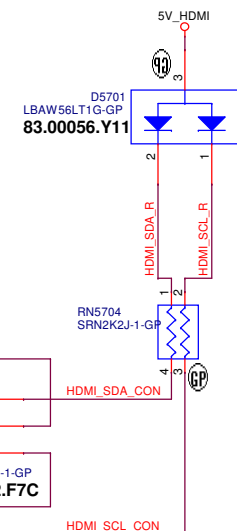
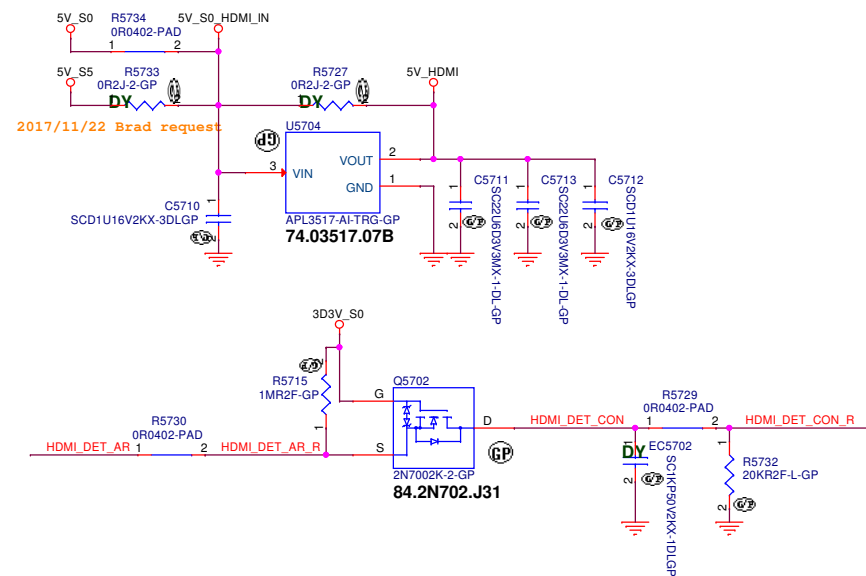
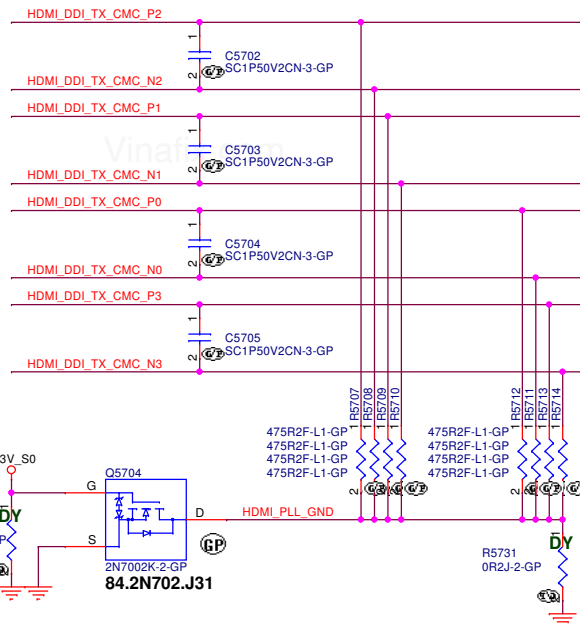
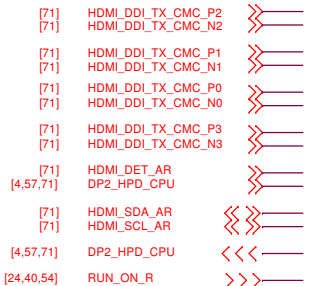
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (LCD/Inverter)**

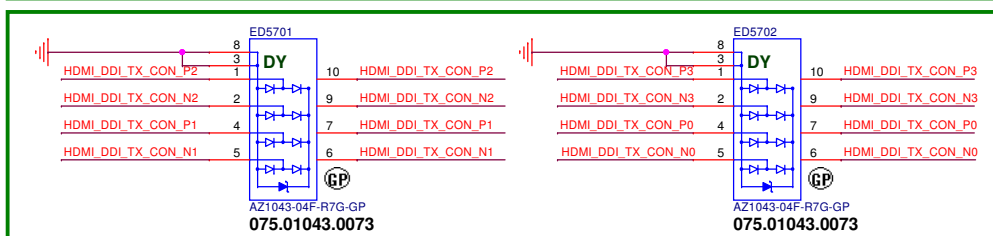
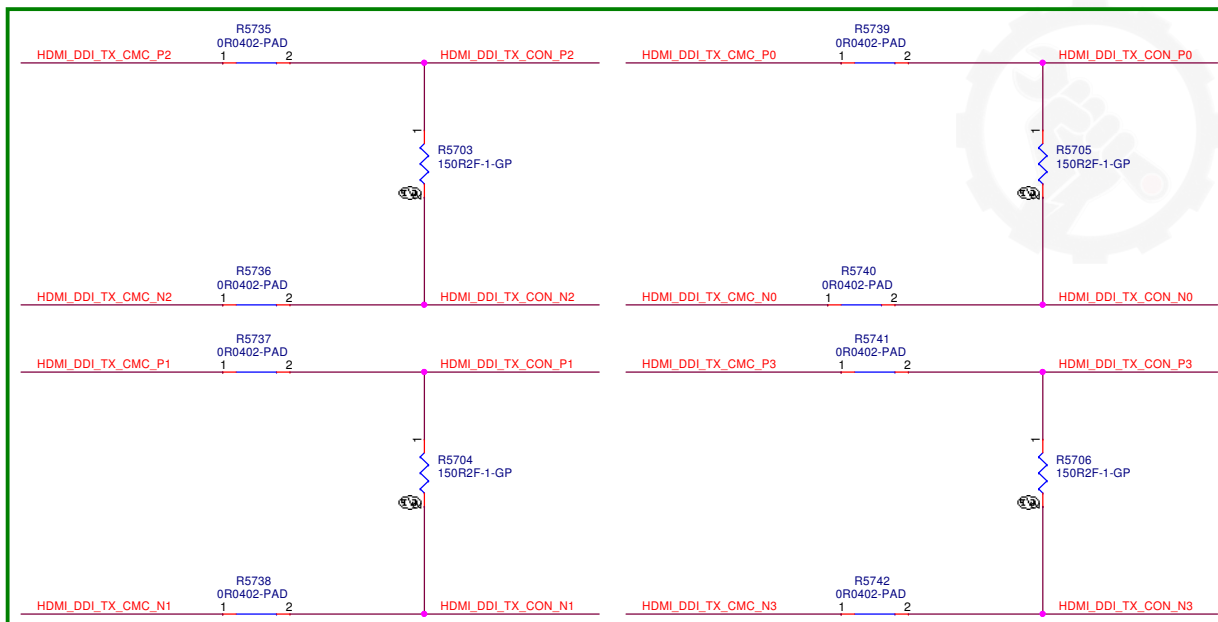
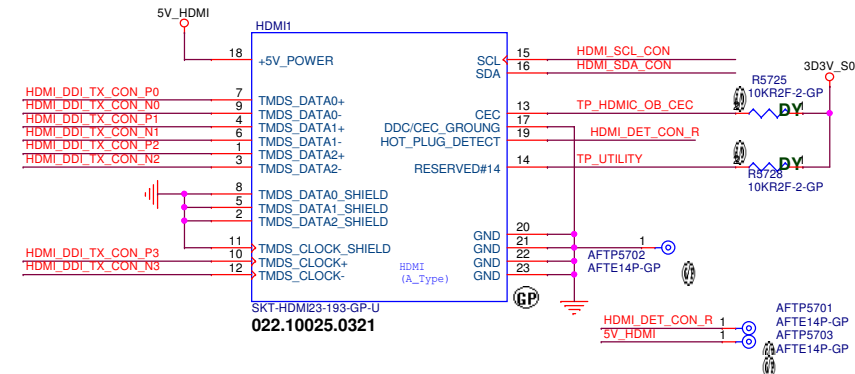
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Date: Friday, February 15, 2019 Sheet 56 of 106

Main Func = HDMI




HDMI CONNECTOR



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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Display (RSVD) DP					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
Date: Friday, February 15, 2019			Sheet	58	of 106

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<Core Design>

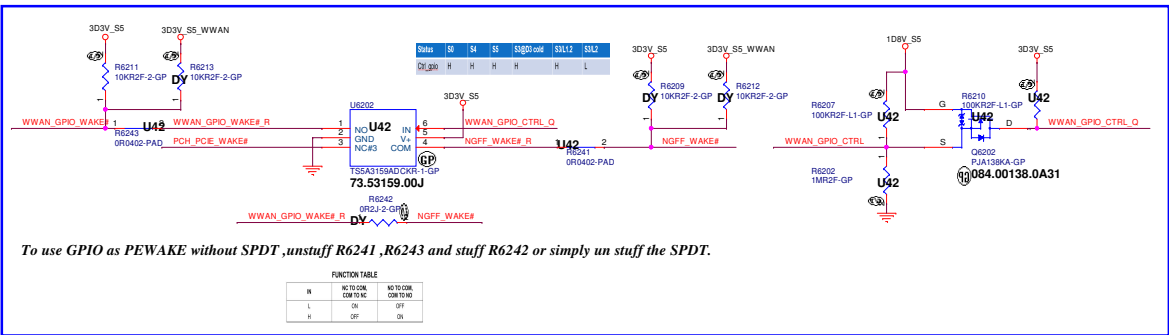
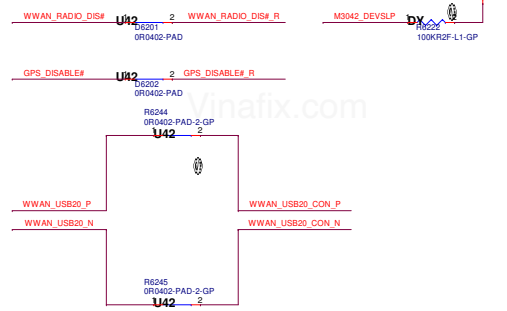
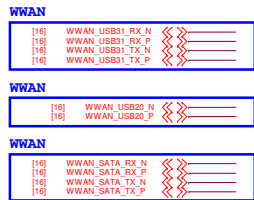
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Display (RSVD) DVI					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
Date: Friday, February 15, 2019			Sheet	59	of 106

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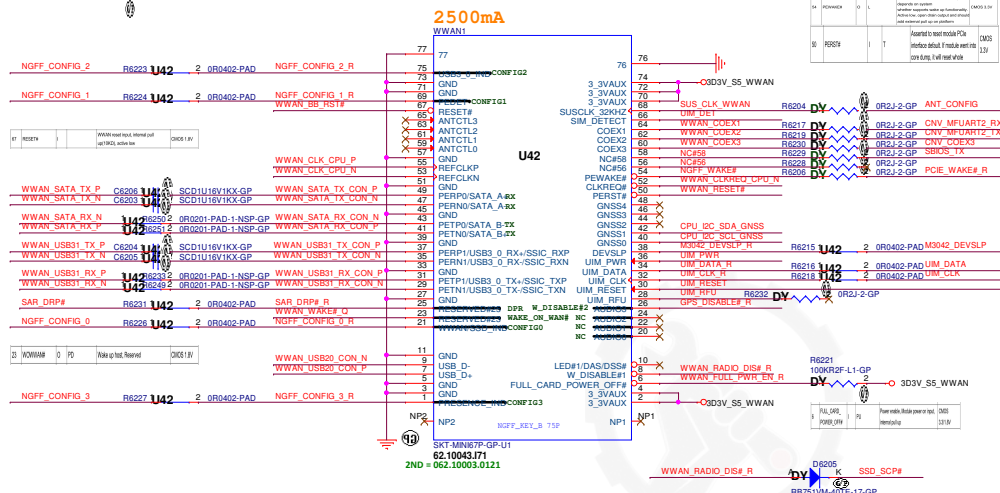
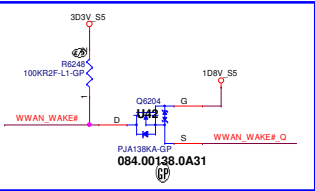
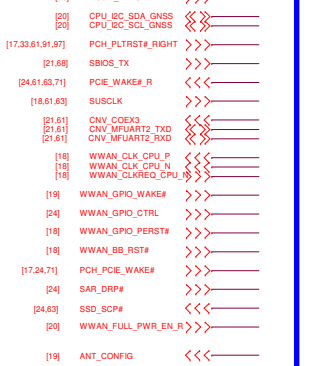
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title INT IO (RSVD)(HDD)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 60 of 106

$NGFF(WWAN/SSD)$ 

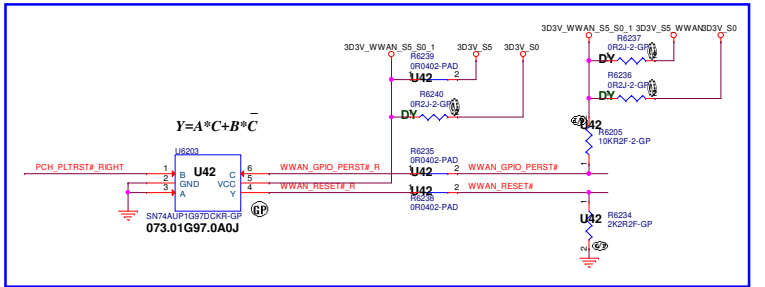
To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



54	PCWATCHDOG	O	L	<p>Assorted to enable up system and disable PCIE link V1.2 to V2.8, depending on system</p> <p>Whether supports wake up functionality, whether it is upper layer control and should enable external pull up on platform</p>	CMOS 1.5V
56	PERST#	I	T	<p>Assorted to reset module PCIe interface before if module went into core dump, it will reset whole</p>	CMOS 1.5V

$$Y=A * C+B * \bar{C}$$



STATE#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M0042_POEIR_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0

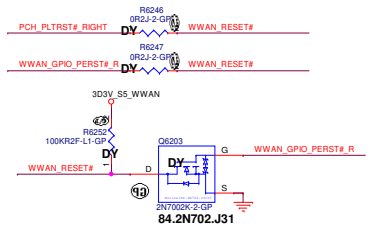


Figure 3-5 Timing Control for Start-up

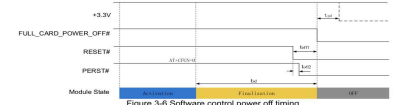
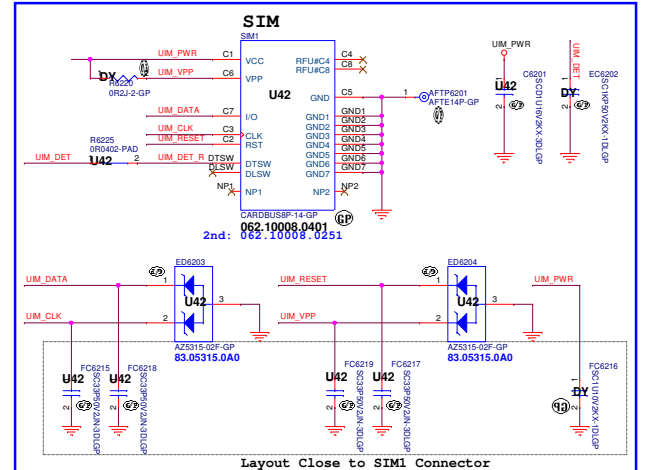


Figure 3-6 Software control power off timing

Index	Minimum	Typical	Notes
t _{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t _{pr}
t _{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t _{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

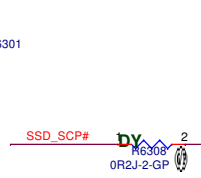
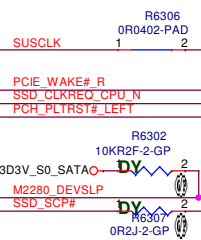
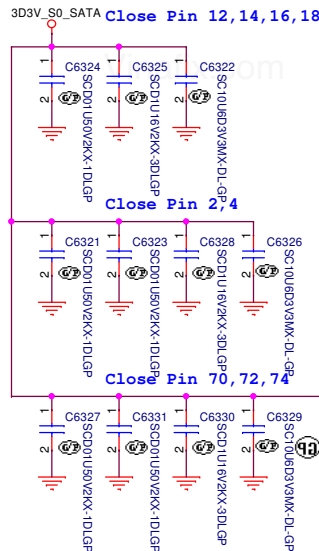
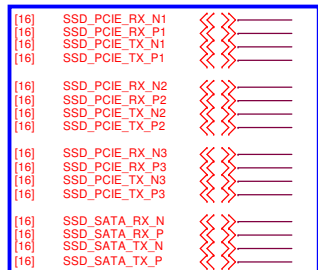
Index	Minimum	Typical	Maxim	Notes
t _{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t _{pd}
t _{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_ON
t _{off2}	0ms	30ms	t _{off1}	PERST# should asserted after RESET#



Layout Close to SIM1 Connector

Main Func = m.2 SSD

SSD



ENG0015277

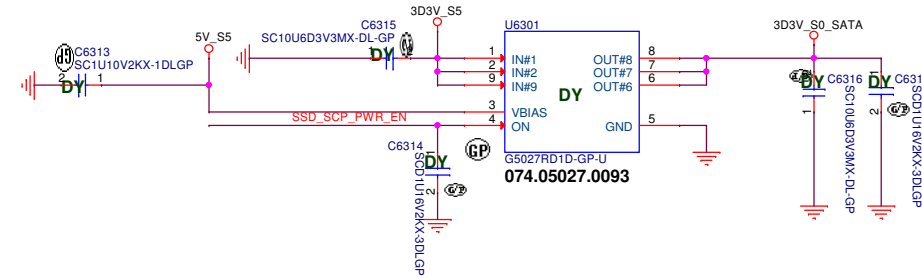
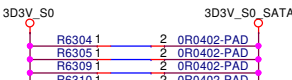
SKT-NGFF75P-203-GP
062.10003.00Z1
2nd: 062.10003.01A1

6.5.4.6

PCH PCI Express* Controller Lane Reversal

For each PCH PCIe* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe* configurations

2800mA



PEDET	0	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	0V/NC
L		SATA	
H		PCI-E	

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF	None	None

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
58	N/C	Connector Key	57
56	N/C	Connector Key	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKP	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	REFCLKN	51
50	PERST# (O)(0/3.3V) or N/C	GND	49
48	N/C	PETp0/SATA-A+	47
44	N/C	PETn0/SATA-A-	45
42	N/C	GND	43
40	N/C	PERp0/SATA-B-	41
38	DEVSLP (O)	PERn0/SATA-B+	39
36	N/C	GND	37
34	N/C	PETp1	35
32	N/C	PETn1	33
30	N/C	GND	31
28	N/C	PERp1	29
26	N/C	PERn1	27
24	N/C	GND	25
22	N/C	PETp2	23
20	N/C	PETn2	21
18	3.3V	GND	19
16	3.3V	PERp2	17
14	3.3V	PERn2	15
12	3.3V	GND	13
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PETp3	11
8	N/C	PETn3	9
6	N/C	GND	7
4	3.3V	PERp3	5
2	3.3V	PERn3	3
		GND	1

<Core Design>



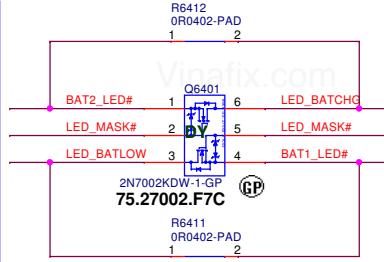
Title INT IO (SSD M.2/ eMMC)

Size A3 Document Number Bandon / NorthBay 13" Rev X00

Date: Friday, February 15, 2019 Sheet 63 of 106

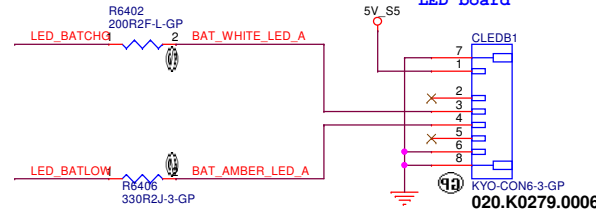
Main Func = LED/HALL/Button

[24] BAT2_LED# >>>
 [24] BAT1_LED# >>>
 [24,32] LED_MASK# >>>
 [24,66,68] KBC_PWRBTN# <<<
 [24,55,67] LID_CL_SIO#_R <<<
 [24,67] LID_CL_SIO_TAB#_R >>>
 [24] BREATH_LED# <<<
 [24,92] FPR_DET# >>>
 [24] M_BIST >>>
 [24,44] ACAV_IN >>>
 [17,24,99] RSMRST#_KBC >>>

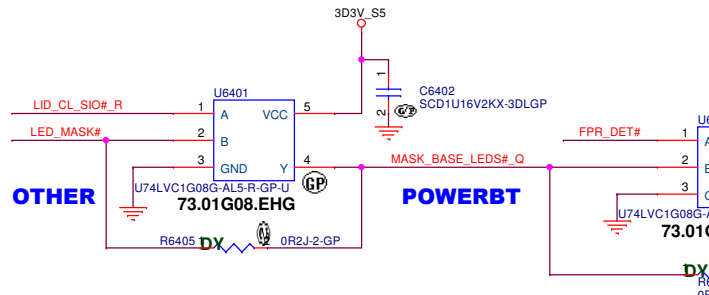
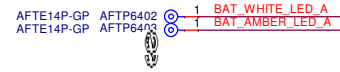


Stealth mode

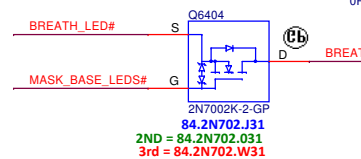
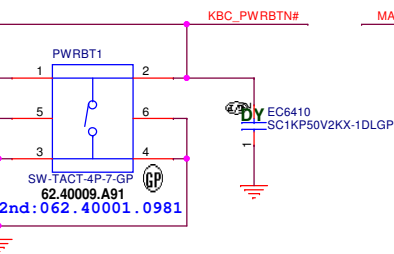
Battery LED2(White LED) LOW acted from KBC GPIO



Battery LED1(Orange LED) LOW acted from KBC GPIO

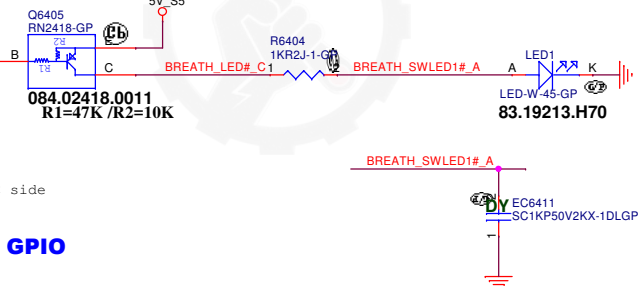


POWER BUTTON

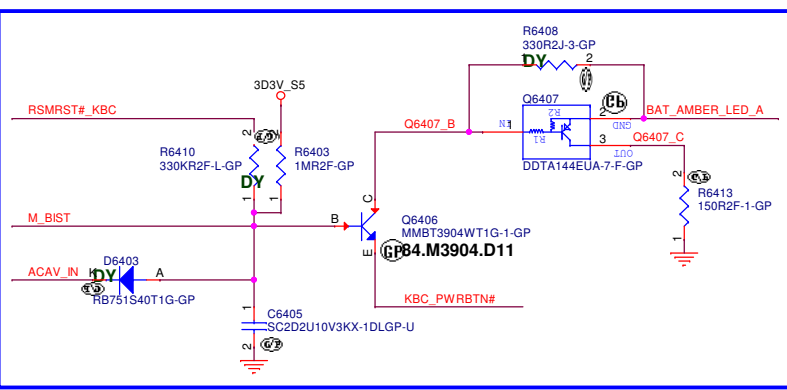


Resistor already reserve on EC side

Power LED LOW acted from KBC GPIO



M-BIST



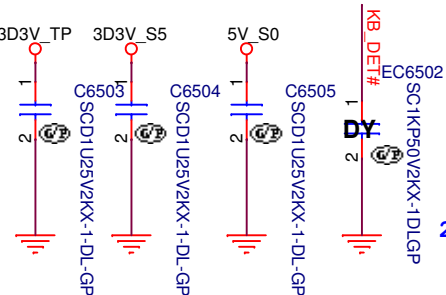
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DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

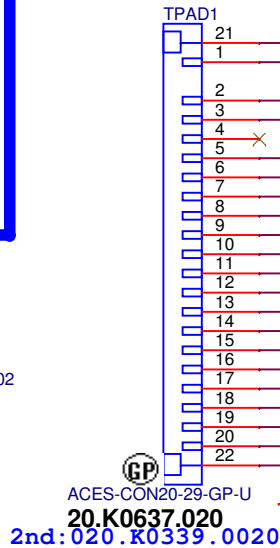
Title LED / Button / Power Button		
Size Custom	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019	Sheet 64	of 106

Main Func = Key Board/Touch Pad

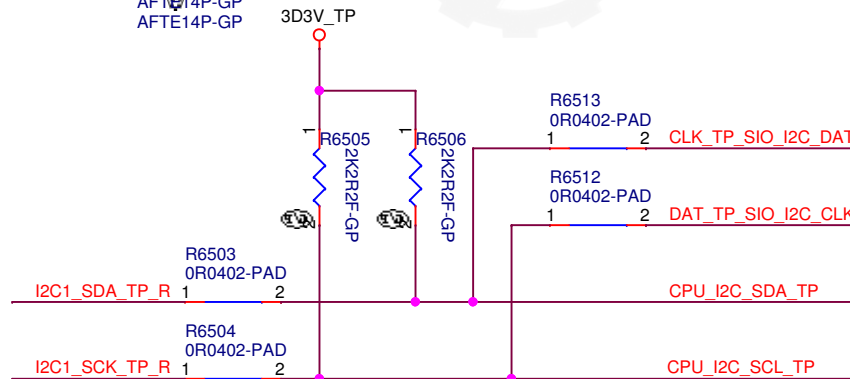
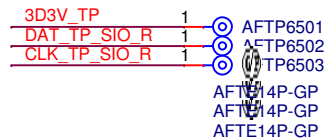
[19]	KB_DET#	<<<
[24]	BC_INT#_ECE1117	<<<
[24]	BC_DAT#_ECE1117	<<<
[24]	BC_CLK#_ECE1117	<<<
[3,24]	TOUCHPAD_INTR#	<<<
[24]	CLK_TP_SIO_I2C_DAT	<<<
[24]	DAT_TP_SIO_I2C_CLK	<<<
[20]	CPU_I2C_SDA_TP	<<<
[20]	CPU_I2C_SCL_TP	<<<
[24]	TP_DISABLE#	>>>



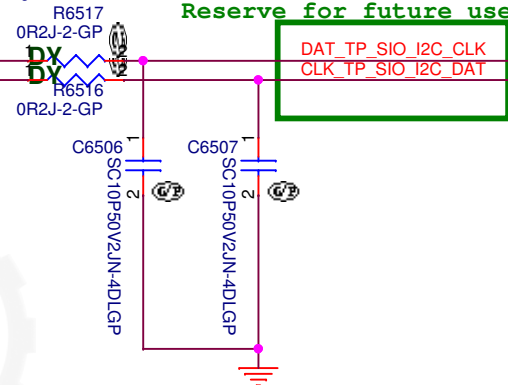
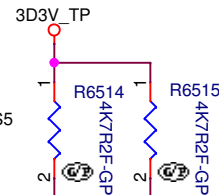
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ACES-CON20-29-GP-U
20.K0637.020
2nd:020.K0339.0020



10mA



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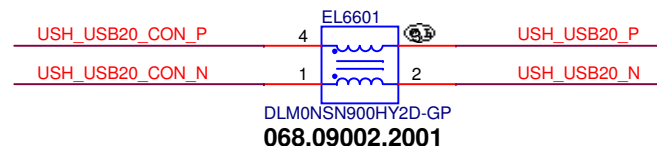
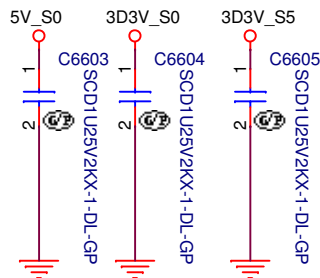
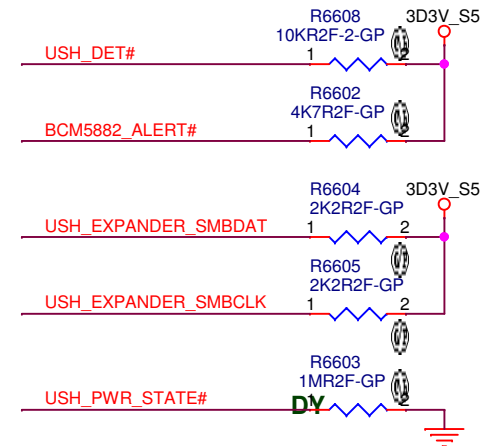
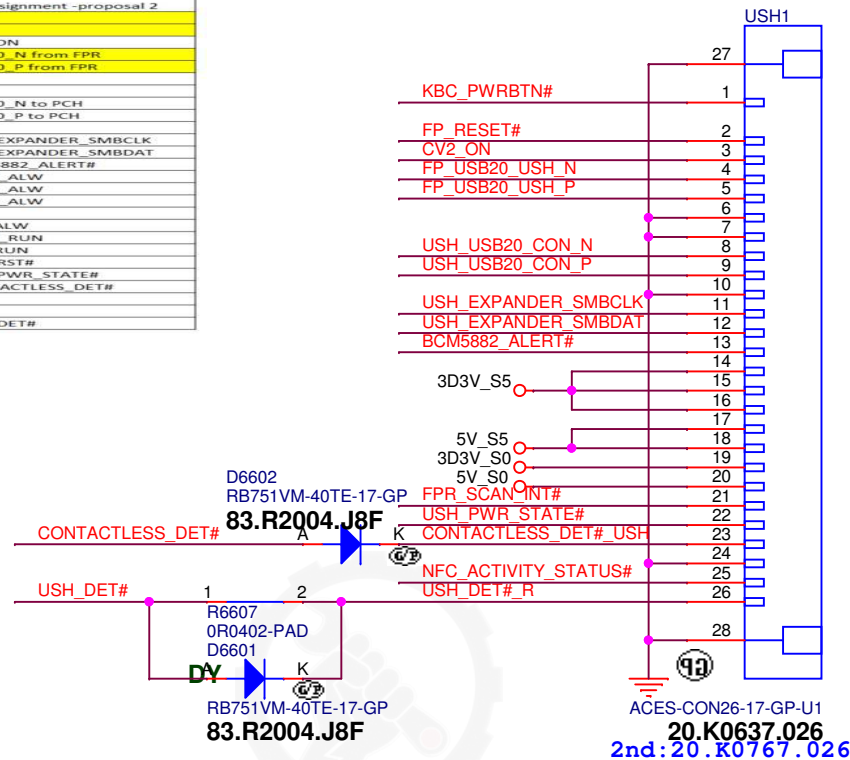
Title			INT IO (KB/TP)	
Size	Document Number	Rev		
A4		Bandon / NorthBay 13"		X00
Date:	Friday, February 15, 2019	Sheet	65	of 106

Main Func = USH BD

USH

[16]	USH_USB20_N	<<>>	
[16]	USH_USB20_P	<<>>	
[24]	CV2_ON	>>>	
[24,69]	USH_EXPANDER_SMBCLK	<<>>	
[24,69]	USH_EXPANDER_SMBDAT	<<>>	
[24]	BCM5882_ALERT#	>>>	
[24]	USH_PWR_STATE#	<<<	
[19]	CONTACTLESS_DET#	<<<	
[24]	USH_DET#	<<<	
[16,92]	FP_USB20_N	<<>>	
[16,92]	FP_USB20_P	<<>>	
[92]	FP_USB20_USH_N	<<>>	
[92]	FP_USB20_USH_P	<<>>	
[24]	NFC_ACTIVITY_STATUS#	<<<	
[92]	FP_RESET#	<<<	
[24,92]	FPR_SCAN_INT#	>>>	
[24,64,68]	KBC_PWRBTN#	>>>	

CV3 module
pin assignment -proposal 2
NC
NC
CV2_ON
USB20_N from FPR
USB20_P from FPR
GND
GND
USB20_N to PCH
USB20_P to PCH
GND
USH_EXPANDER_SMBCLK
USH_EXPANDER_SMBDAT
BCM5882_ALERT#
+3.3V_ALW
+3.3V_ALW
+3.3V_ALW
NC
+5V_ALW
+3.3V_RUN
+5V_RUN
USH_RST#
USH_PWR_STATE#
CONTACTLESS_DET#
GND
GND
USH_DET#



<Core Design>



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Title **IO Board Conn (USH)**

Size A4 Document Number **Bandon / NorthBay 13"** Rev **X00**

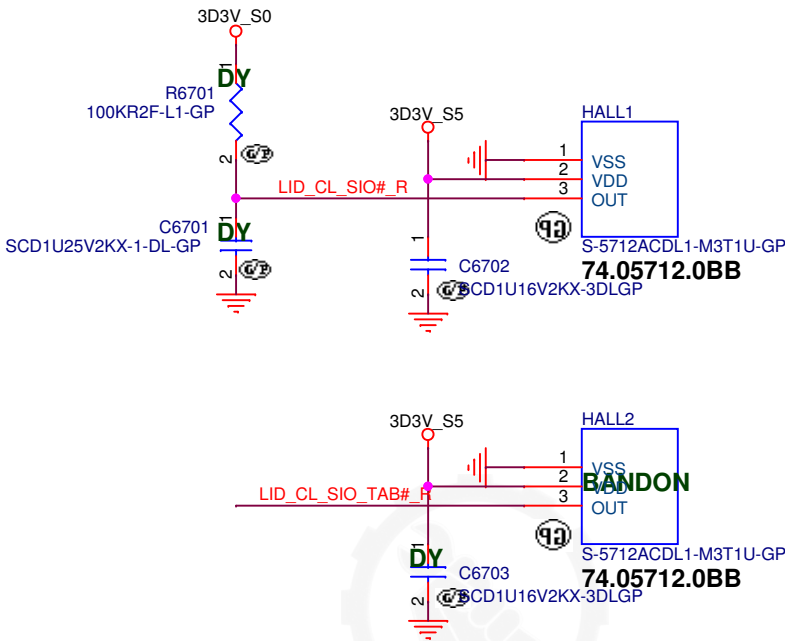
Date: Friday, February 15, 2019 Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)


[24,55,64] LID_CL_SIO#_R << >>—
[24,64] LID_CL_SIO_TAB#_R << >>—

BANDON
TCS40DLR
[074.TCS40.M001]

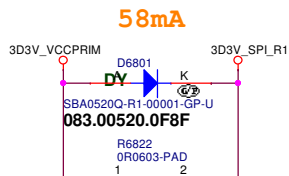
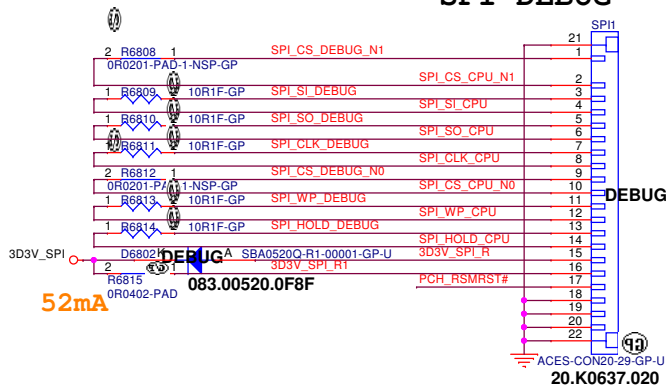
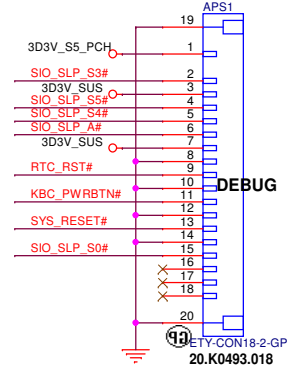
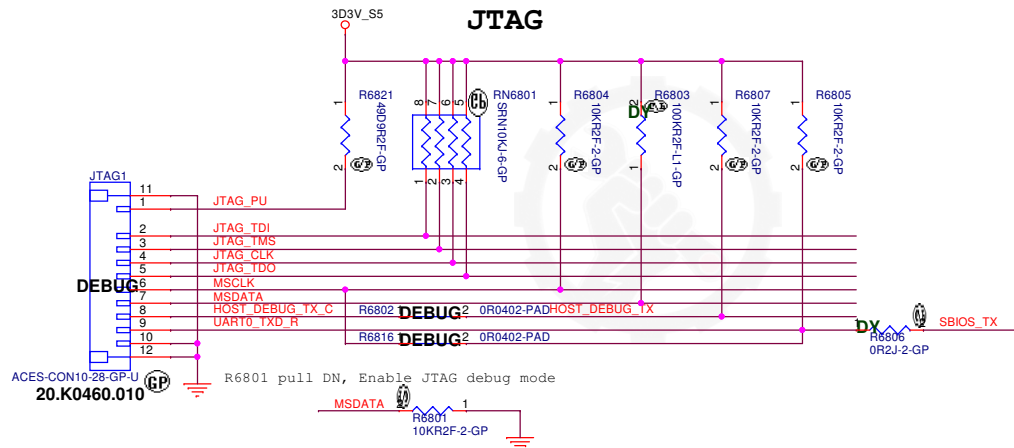
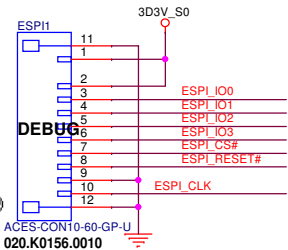
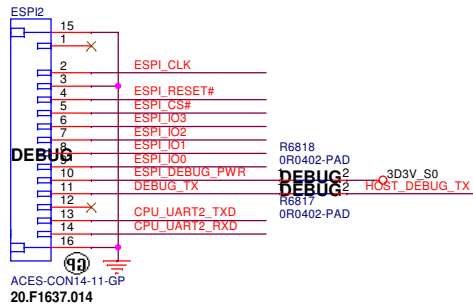
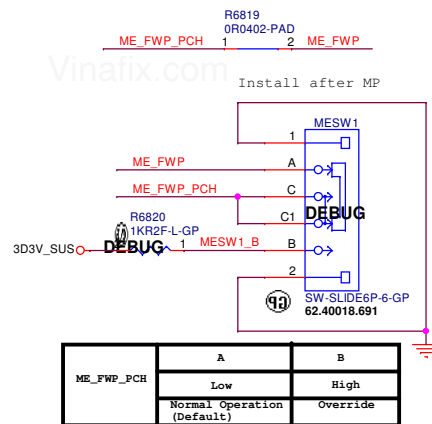
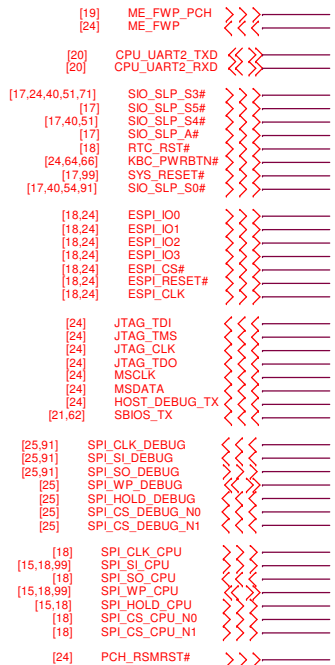
NORTHBAY
APX8131A
[074.08131.007B]



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Title Sensor (Hall-Sensor)			
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Main Func = Debug



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Title	Author	Year	Journal	Volume	Page
...

Debug (LPC debug)

Size

Document Number

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Rev

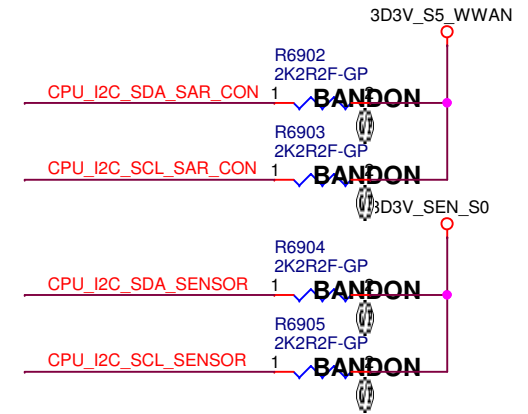
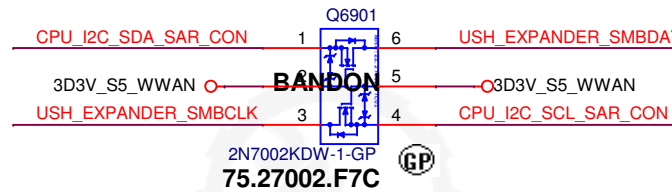
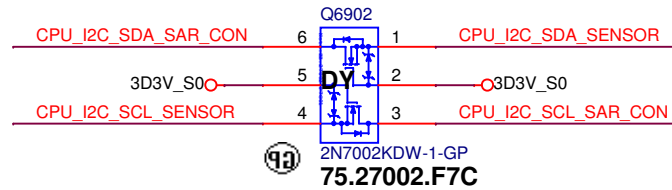
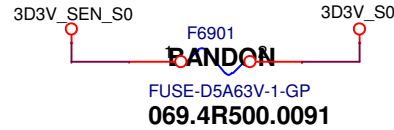
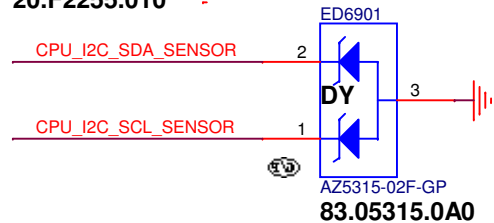
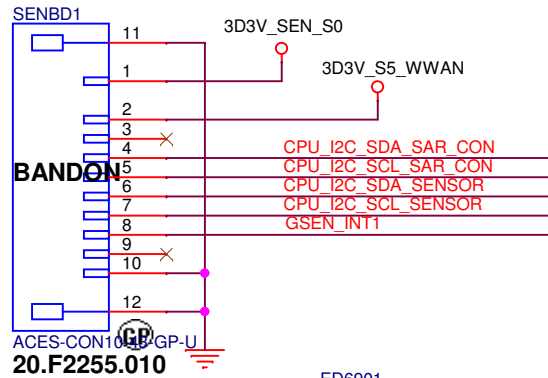
Date: Friday, February 15, 2019

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106

Main Func = Sensor (E-compass/A+Gyro/SAR)

[20] GSEN_INT1 <<< _____
[20,70] CPU_I2C_SDA_SENSOR <<< _____
[20,70] CPU_I2C_SCL_SENSOR <<< _____
[24,66] USH_EXPANDER_SMBDAT <<< _____
[24,66] USH_EXPANDER_SMBCLK <<< _____



<Core Design>

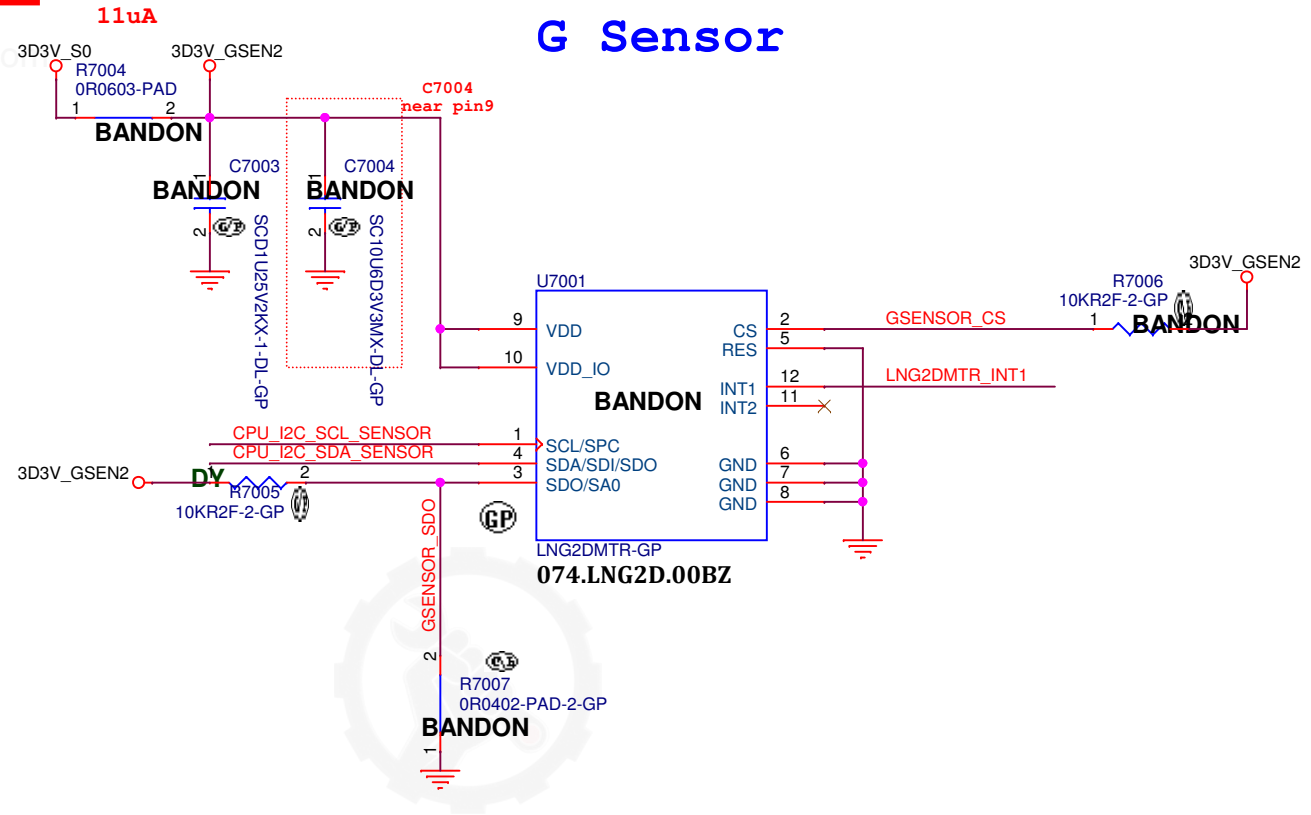


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Title				Sensor (GYROSCOPE/PRESSUE/ALS)			
Size		Document Number			Rev		
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Main Func = G-sensor

```
[20,69] CPU_I2C_SDA_SENSOR
[20,69] CPU_I2C_SCL_SENSOR
[20]    LNG2DMTR_INT1
```



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Title

Sensor (G-sensor)

Size
A4

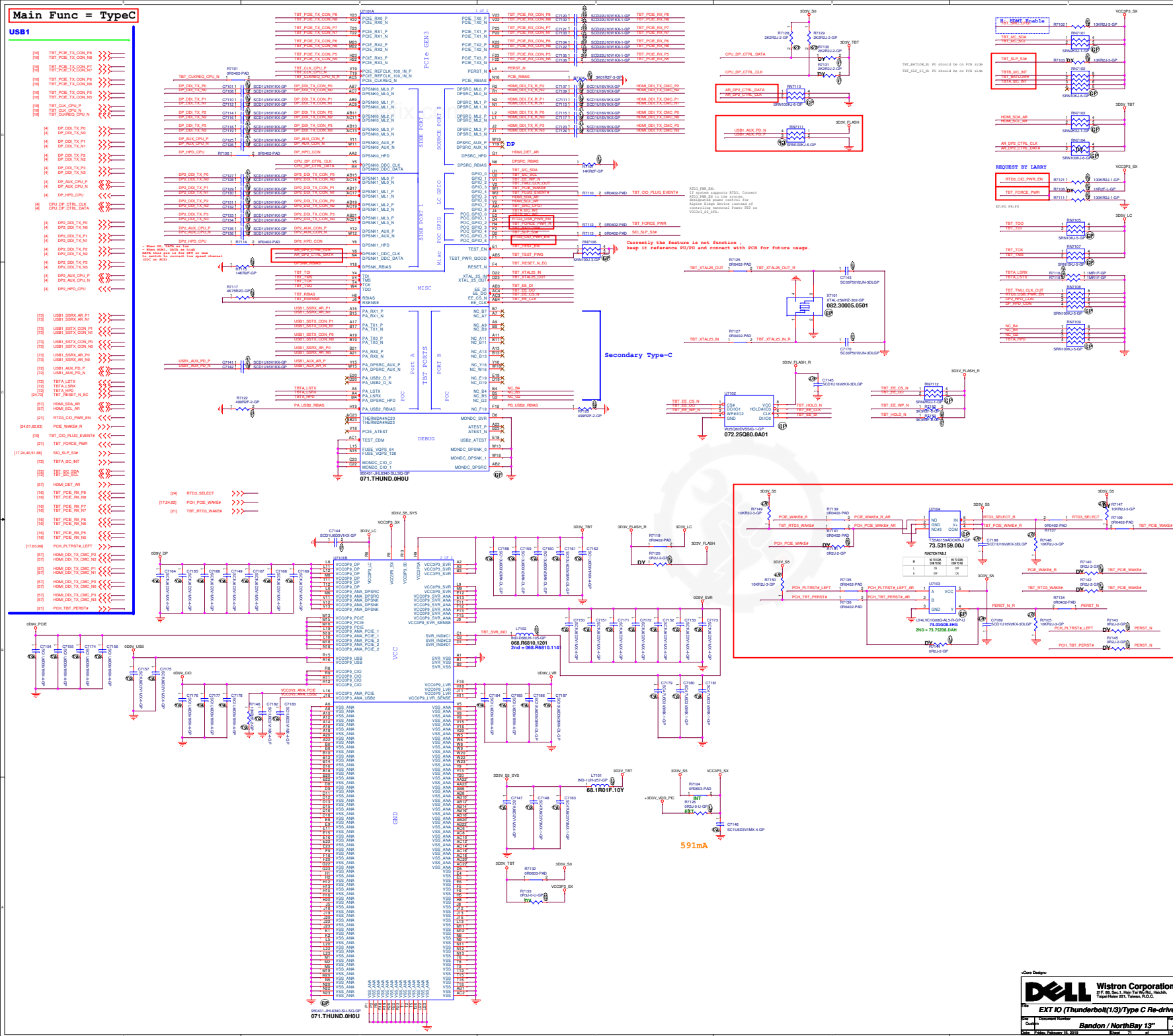
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Bandon / NorthBay 13"

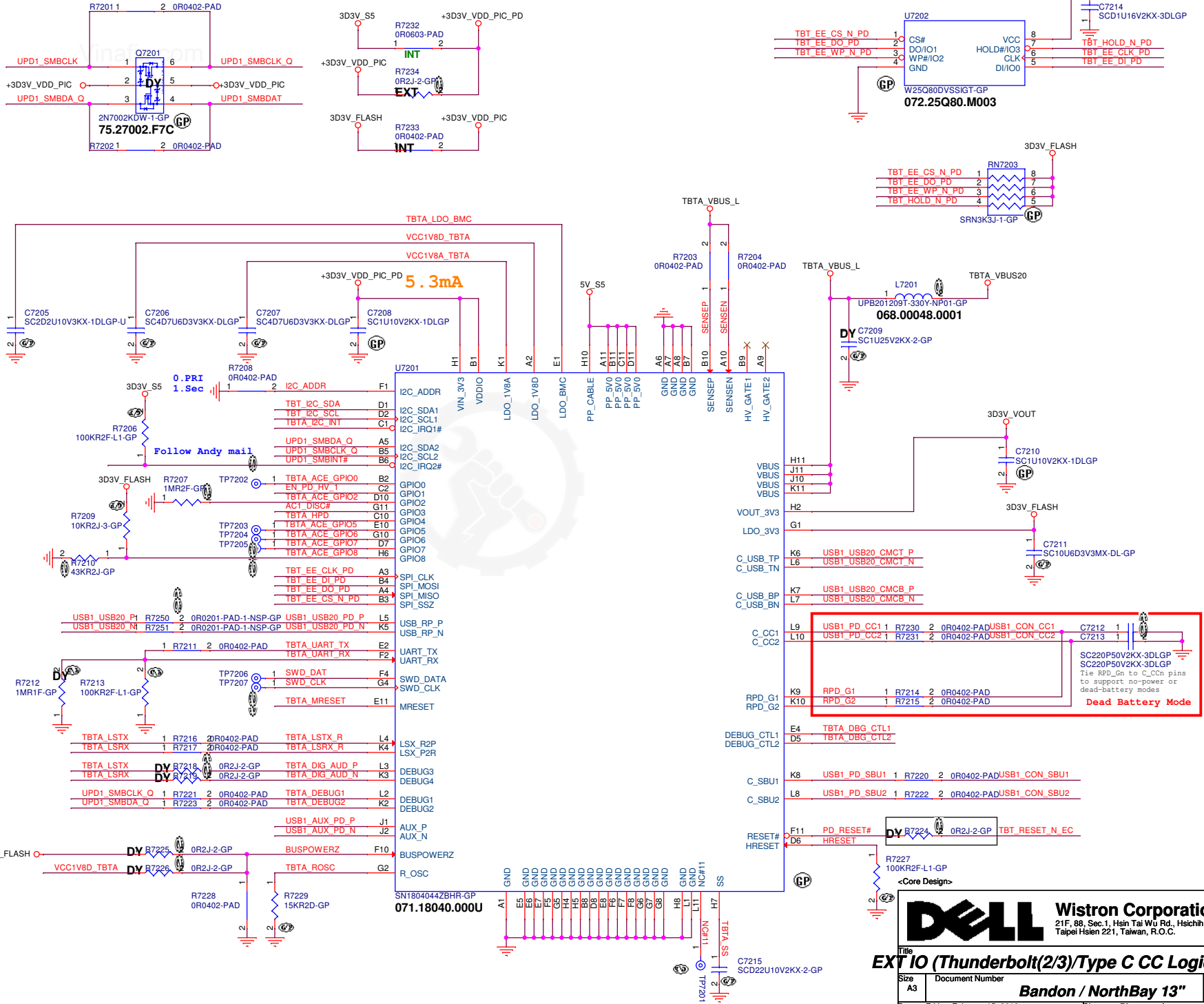
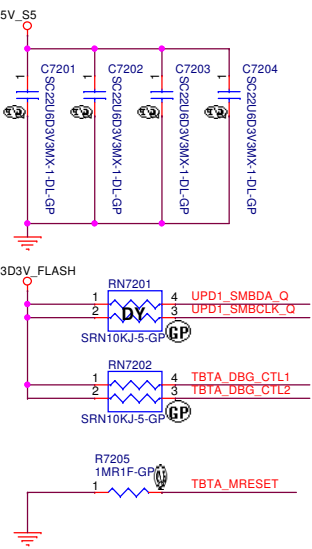
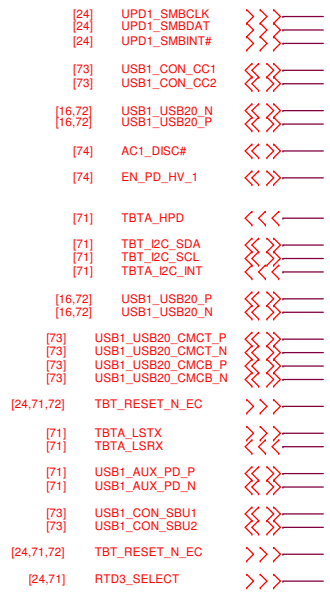
Rev
X00

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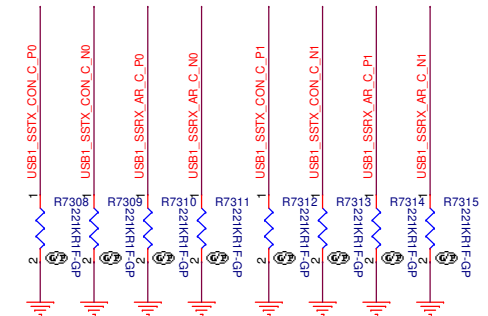
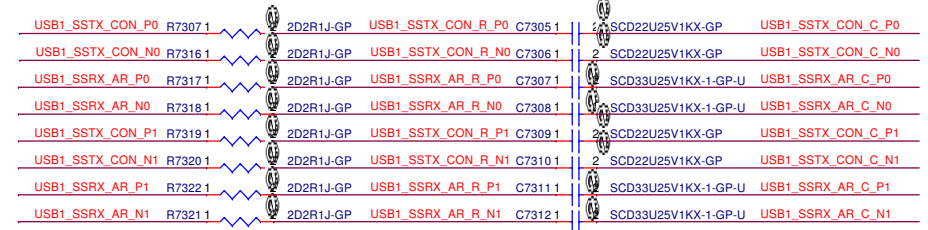
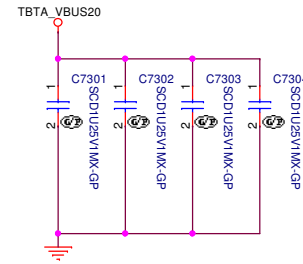


Main Func = TypeC



For Layout Swap A&B Connection

[71]	USB1_SSTX_CON_P0	⋮
[71]	USB1_SSTX_CON_P0	⋮
[71]	USB1_SSTX_CON_P1	⋮
[71]	USB1_SSTX_CON_P1	⋮
[71]	USB1_SSRX_AR_P0	⋮
[71]	USB1_SSRX_AR_P0	⋮
[71]	USB1_SSRX_AR_P1	⋮
[71]	USB1_SSRX_AR_P1	⋮
[72]	USB1_USB20_CMCT_P	⋮
[72]	USB1_USB20_CMCT_P	⋮
[72]	USB1_USB20_CMCT_P	⋮
[72]	USB1_USB20_CMCT_P	⋮
[72]	USB1_CON_CC1	⋮
[72]	USB1_CON_CC2	⋮
[72]	USB1_CON_SBU1	⋮
[72]	USB1_CON_SBU2	⋮



Title **EXT IO (Thunderbolt(3/3)/Type C Conn)**


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Title EXT IO (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU (RSVD) (PEG 1/5)					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title			GPU (RSVD) (DIGITAL 2/5)		
Size A4	Document Number			Rev X00	
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (VRAM 3/5)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 78 of 106

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (RSVD) (GPIO 4/5)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
Date: Friday, February 15, 2019		Sheet 79 of	106

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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU (RSVD) (PWR/GND 5/5)					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (VRAM1,2 1/4)		
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (VRAM3,4 2/4)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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<Core Design>

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Title GPU (RSVD) (VRAM5,6 3/4)					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
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<Core Design>

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Title					
GPU (RSVD) (VRAM7,8 4/4)					
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<Core Design>

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Title GPU (RSVD) (VGA_CORE)					
Size A4		Document Number Bandon / NorthBay 13"			Rev X00
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<Core Design>

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Title GPU (RSVD) (Sequence)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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<Core Design>

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Title GPU (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
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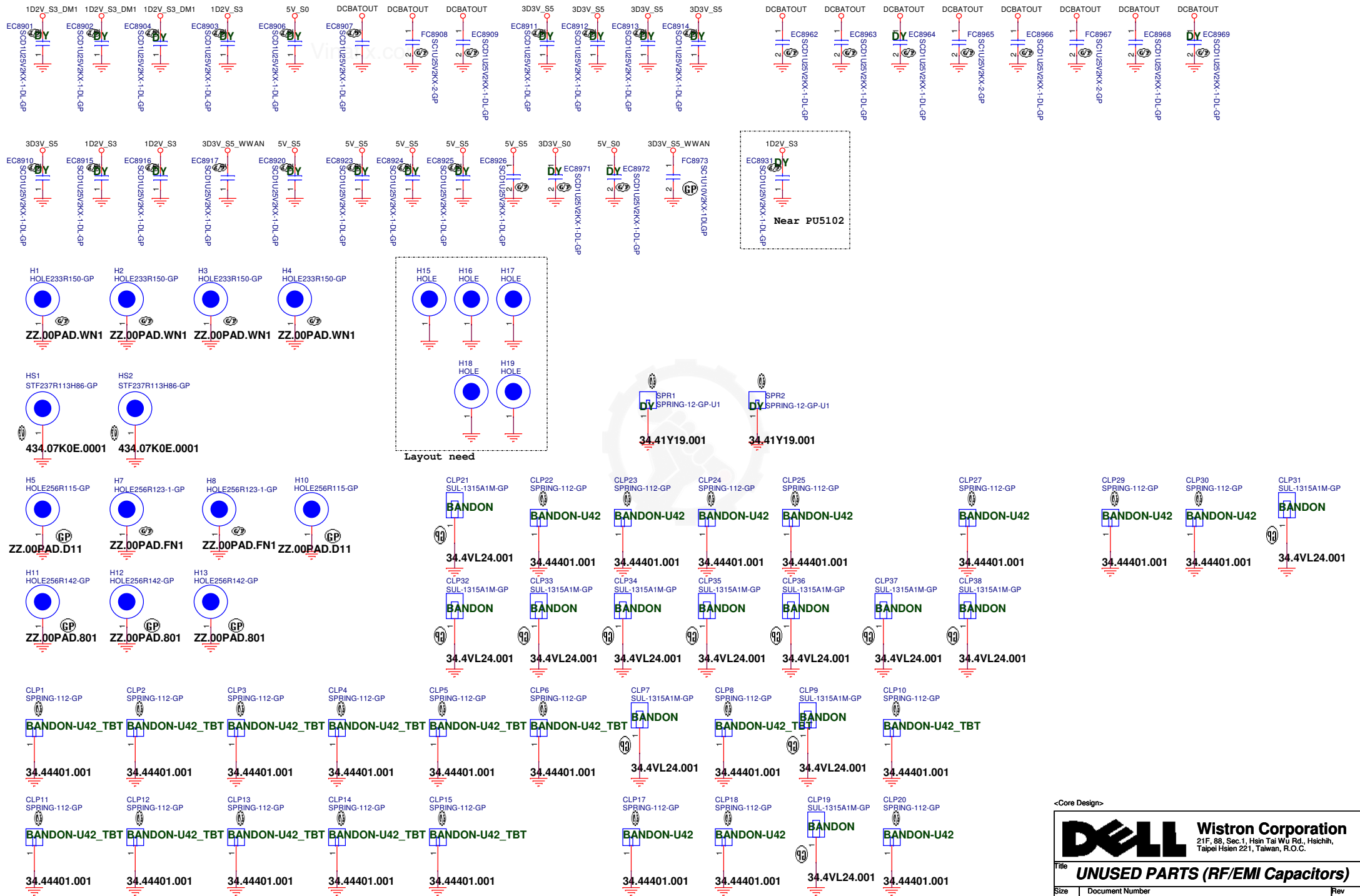
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<Core Design>

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Title UNUSED PARTS (RSVD)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Main Func = EMC/ RF



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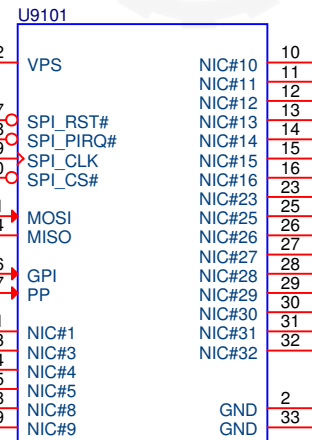
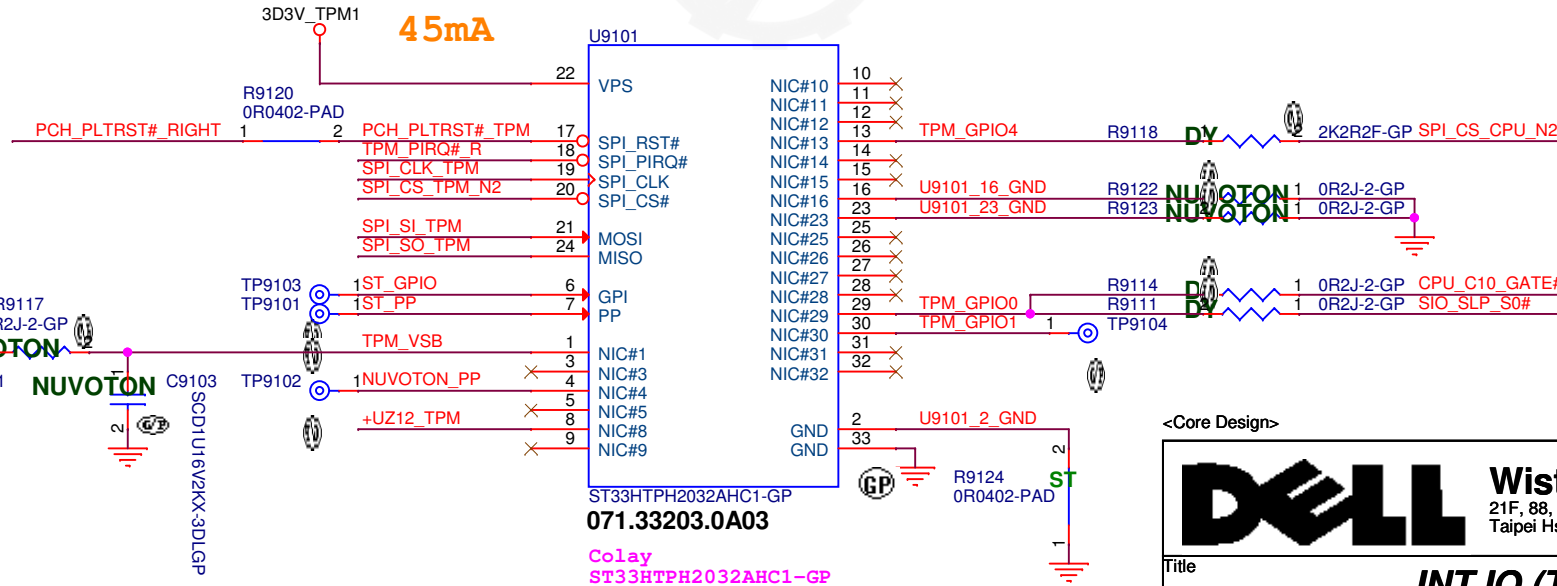
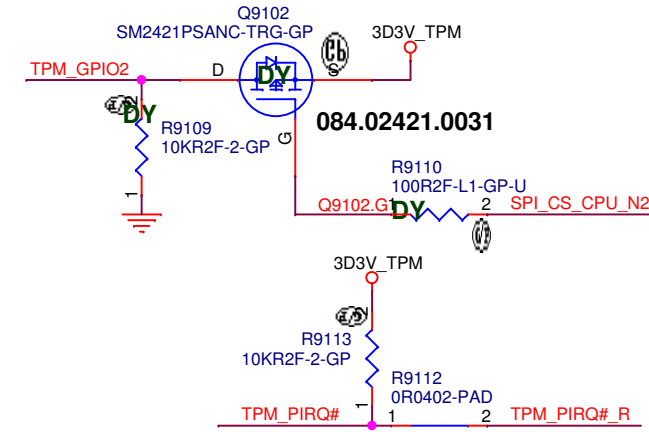
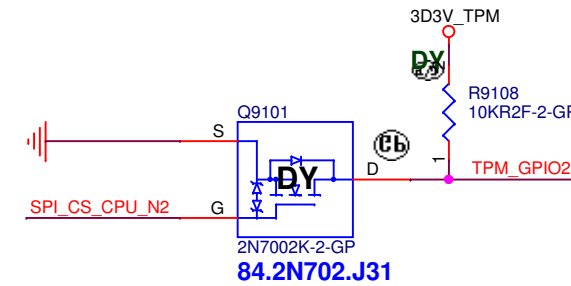
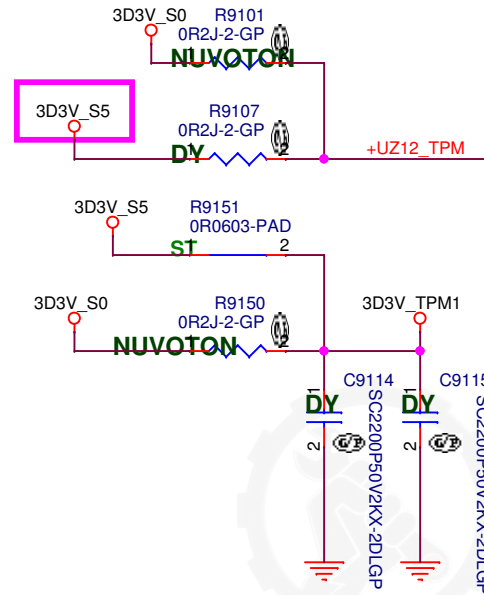
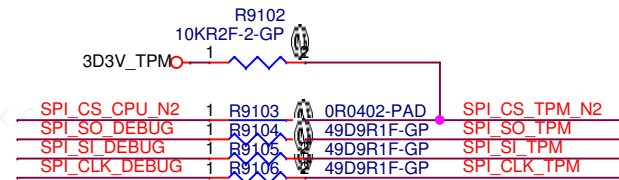
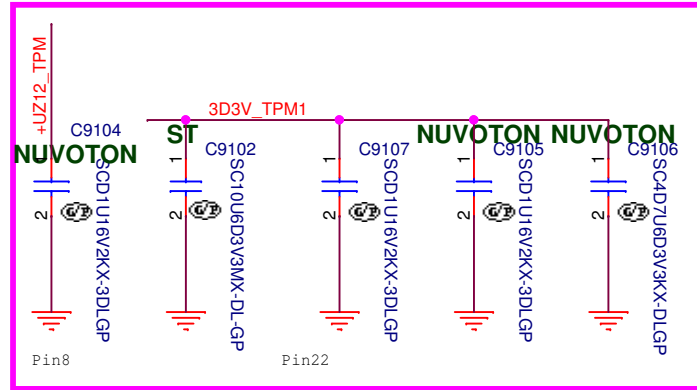


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Title INT IO (RSVD) (NFC)		
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Main Func = TPM

[20]	TPM_PIRQ#	
[17,40,54,68]	SIO_SLP_S0#	
[17,33,61,62,97]	PCH_PLTRST#_RIGHT	
[25,68]	SPI_CLK_DEBUG	
[25,68]	SPI_SI_DEBUG	
[25,68]	SPI_SO_DEBUG	
[18]	SPI_CS_CPU_N2	
[21,24,40,54]	CPU_C10_GATE#	



ST33HTPH2032AHC1-GP
071.33203.0A03

Colay
ST33HTPH2032AHC1-GP
071.33203.0A03
NPCT750JAAYX-1-GP
071.00750.M001

<Core Design>



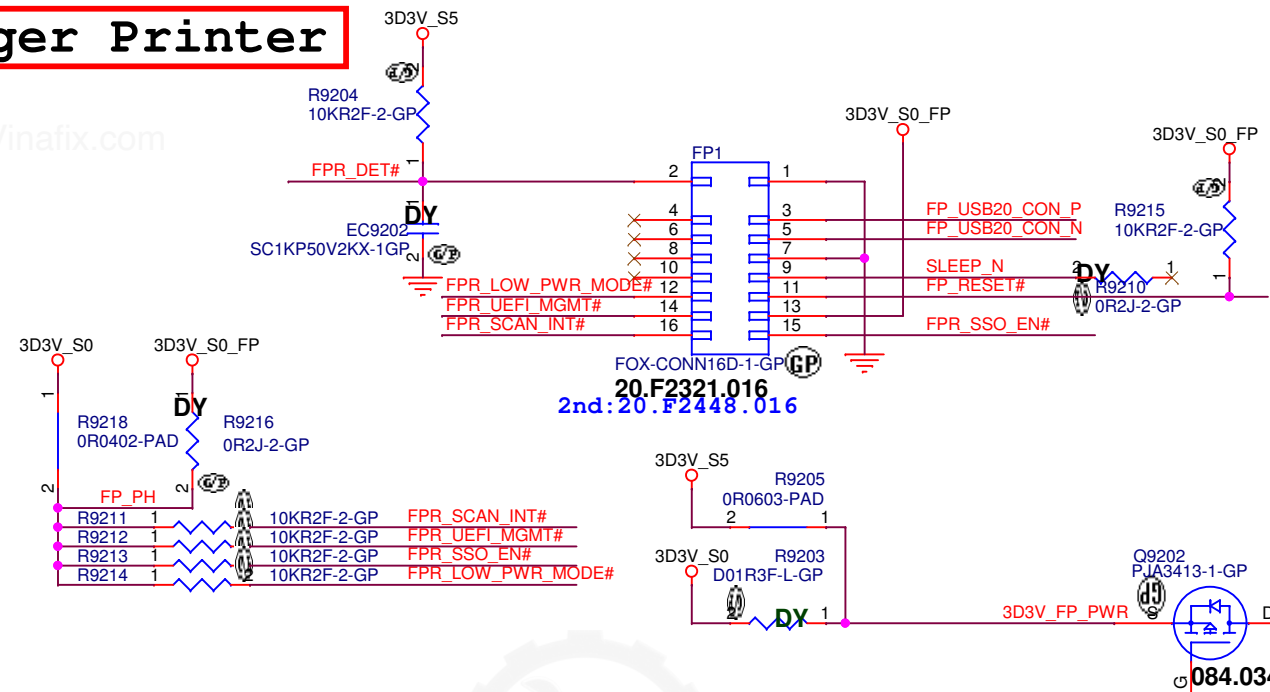
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Taipei Hsien 221, Taiwan, R.O.C.

Title			INT IO (TPM)	
Size	Document Number	Bandon / NorthBay 13"		Rev
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Main Func = Finger Printer

- [16] FP_USB20_N
- [16] FP_USB20_P
- [24,64] FPR_DET#
- [66] FP_USB20_USH_N
- [66] FP_USB20_USH_P
- [24] FPR_PWR_EN#
- [24,66] FPR_SCAN_INT#
- [24] FPR_SSO_EN#
- [24] FPR_UEFI_MGMT#
- [24] FPR_LOW_PWR_MODE#
- [66] FP_RESET#

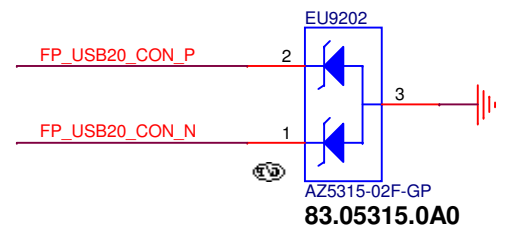
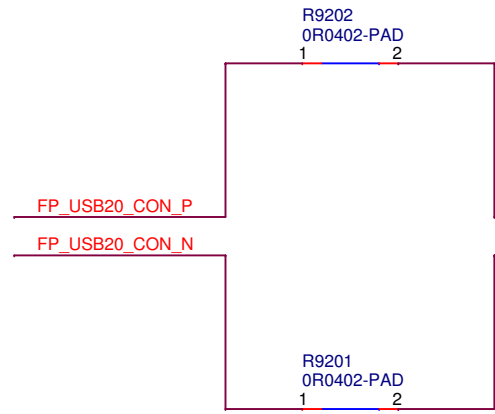
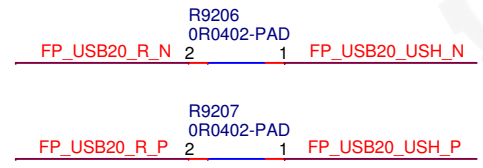
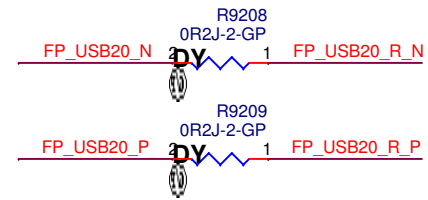
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Pin 1	GND
Pin 2	FPR_DET(GND)
Pin 3	USB_DP
Pin 4	NA
Pin 5	USB_DM
Pin 6	NA
Pin 7	GND
Pin 8	NA
Pin 9	RESERVED
Pin 10	NA
Pin 11	FP_RESET#
Pin 12	LOW POW MODE#
Pin 13	VDD CHICLET
Pin 14	UEFI_MGMT#
Pin 15	SSO_EN#
Pin 16	FPR_SCAN_INTR#

PCH

USH



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Title

INT IO (Finger Printer)

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title EXT IO (RSVD) (Express Card/PCIE slot)					
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Title EXT IO (RSVD) (Smart Card/COM/PS2)		
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Title		Commercial (RSVD) (SW GFX eDP)	
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LAN




10. *Journal of the American Medical Association*, 2000; 284: 2689-2695.



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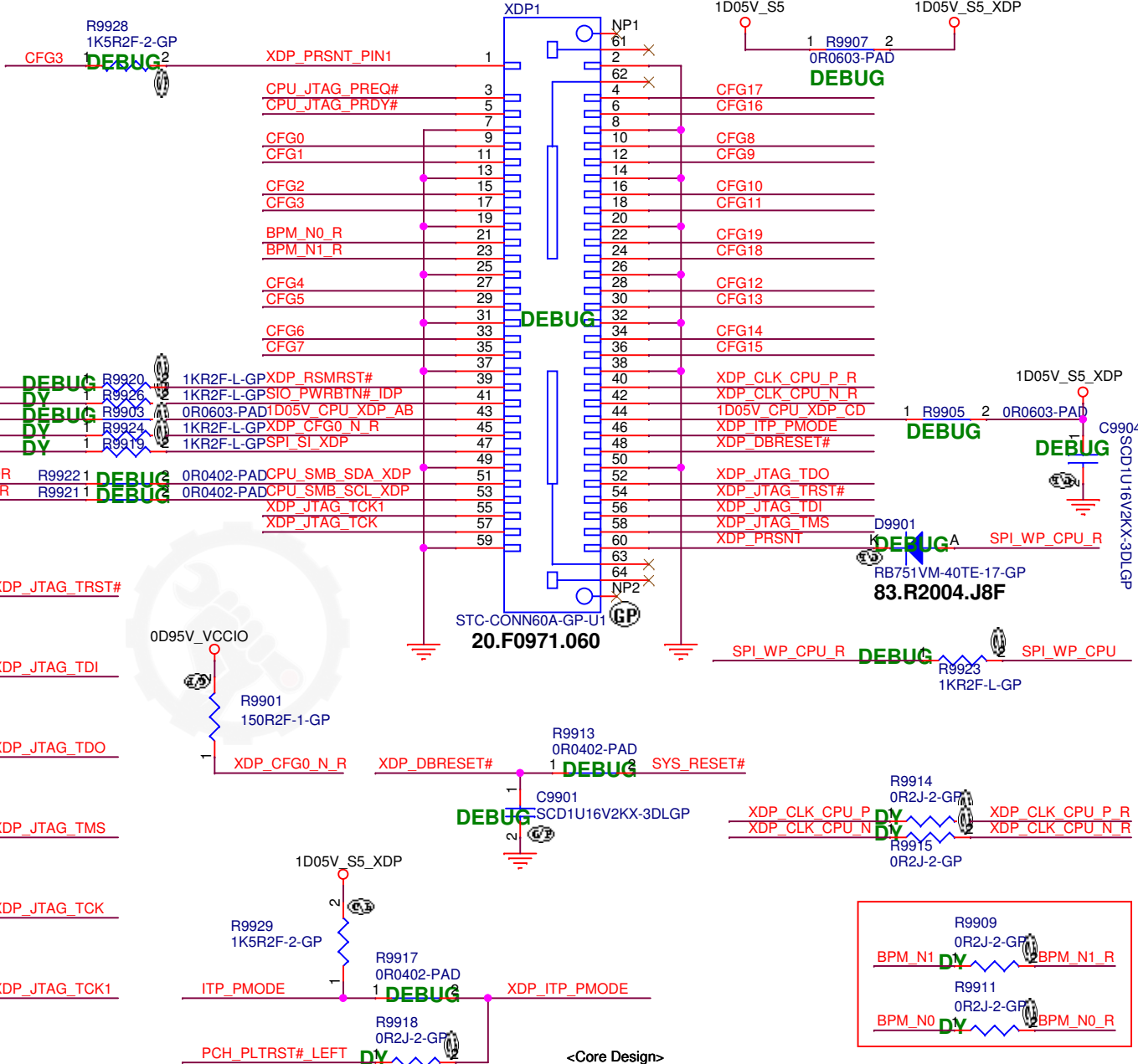
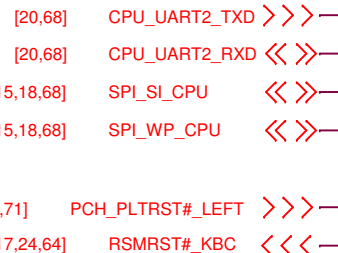
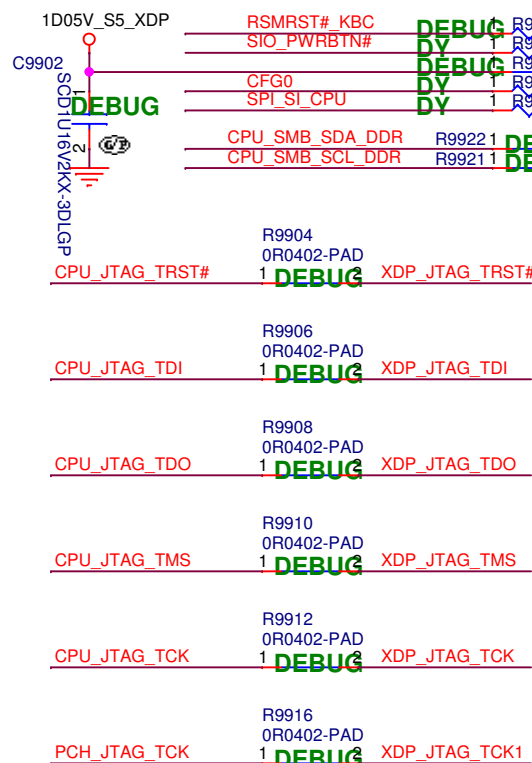
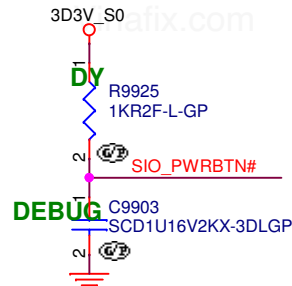


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Title Commercial (LAN Switch)					
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Main Func = Debug (MIPI)

[6] CFG0 >>>-
[6] CFG1 >>>-
[6] CFG2 >>>-
[6] CFG3 >>>-
[6] CFG4 >>>-
[6] CFG5 >>>-
[6] CFG6 >>>-
[6] CFG7 >>>-
[6] CFG8 >>>-
[6] CFG9 >>>-
[6] CFG10 >>>-
[6] CFG11 >>>-
[6] CFG12 >>>-
[6] CFG13 >>>-
[6] CFG14 >>>-
[6] CFG15 >>>-
[6] CFG16 >>>-
[6] CFG17 >>>-
[6] CFG18 >>>-
[6] CFG19 >>>-
[3] BPM_N0 >>>-
[3] BPM_N1 >>>-
[6,15] ITP_PMODE >>>-
[18] XDP_CLK_CPU_N <<<-
[18] XDP_CLK_CPU_P <<<-
[3] PCH_JTAG_TCK <<<-
[3] CPU_JTAG_PRDY# <<<-
[3] CPU_JTAG_PREQ# <<<-
[3] CPU_JTAG_TRST# <<<-
[3] CPU_JTAG_TCK <<<-
[3] CPU_JTAG_TDI <<<-
[3] CPU_JTAG_TDO <<<-
[3] CPU_JTAG_TMS <<<-
[17,68] SYS_RESET# >>>-
[17,24] SIO_PWRBTN# >>>-
[12,13,18] CPU_SMB_SCL_DDR <<<-
[12,13,18] CPU_SMB_SDA_DDR <<<-
[17,63,71] PCH_PLTRST#_LEFT >>>-
[17,24,64] RSMRST#_KBC <<<-



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Title			Debug (XDP debug)	
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

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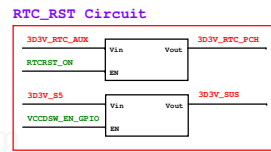
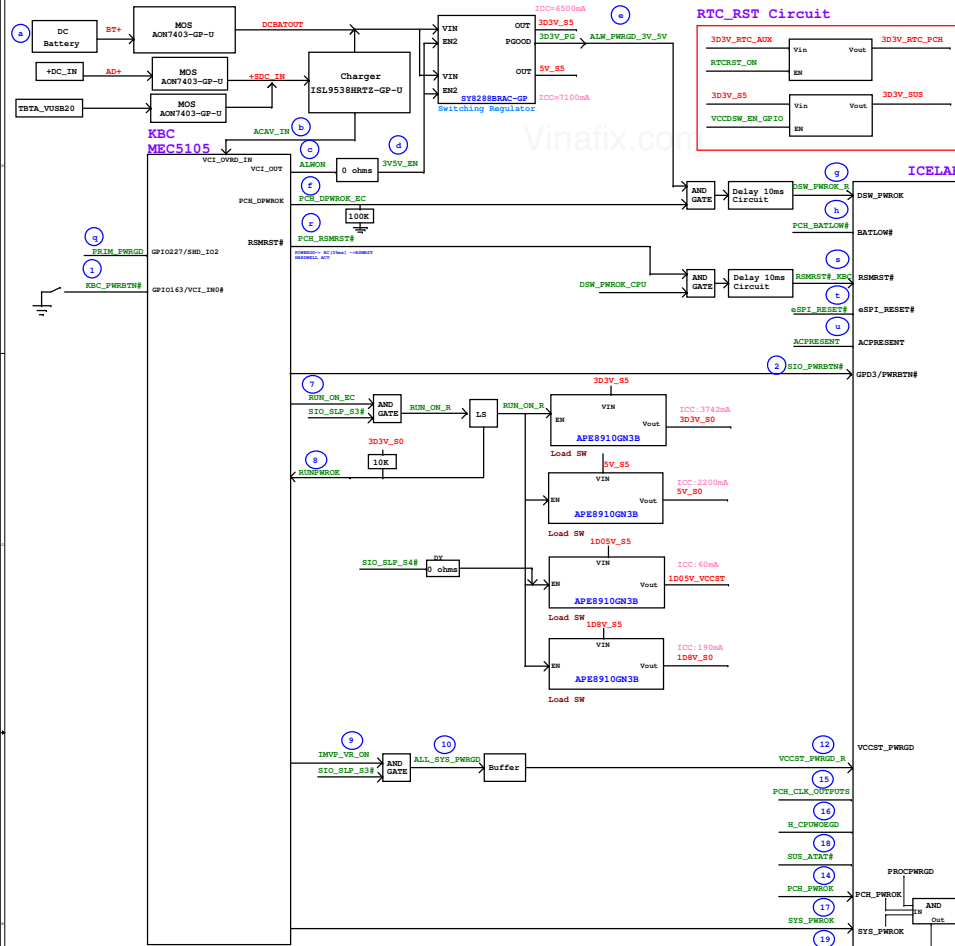
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X00

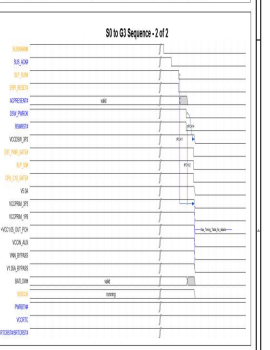
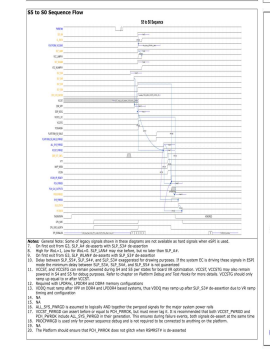
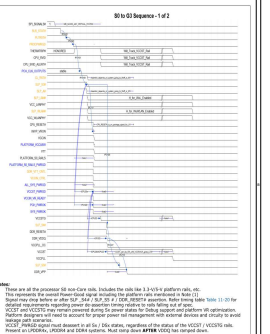
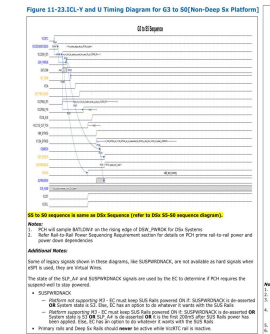
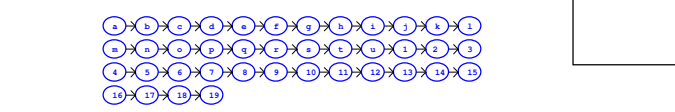
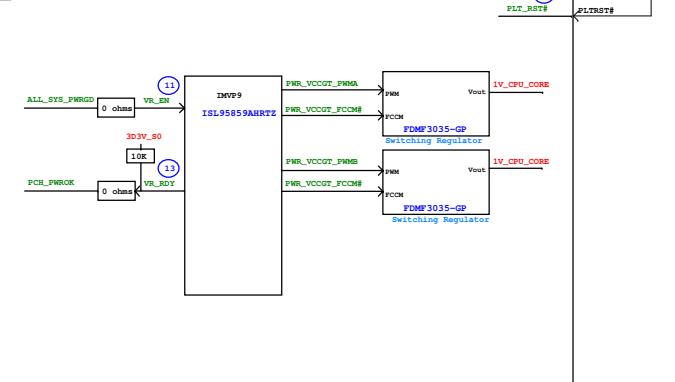
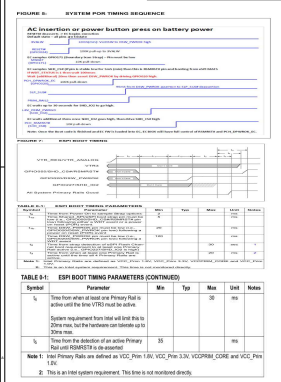
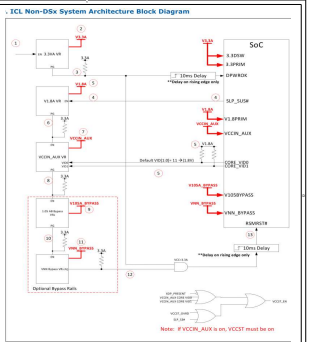
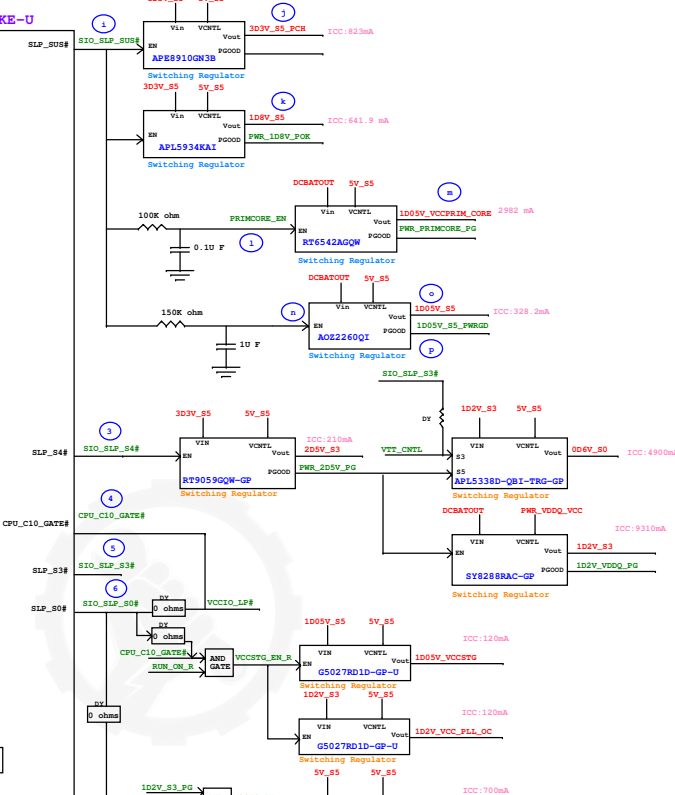
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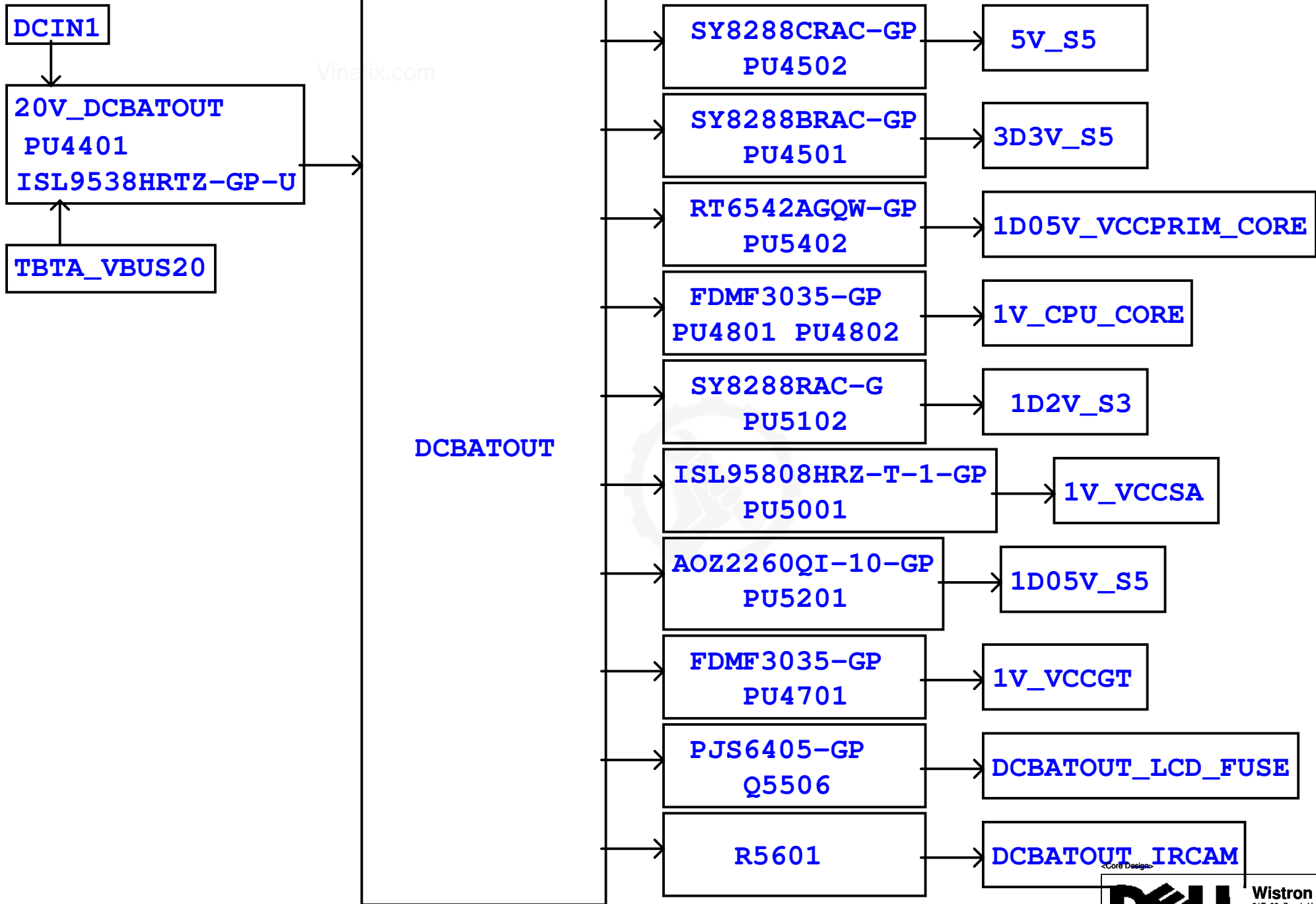
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Bandon /NorthBay Power up sequence diagram (deep Sx Platform)

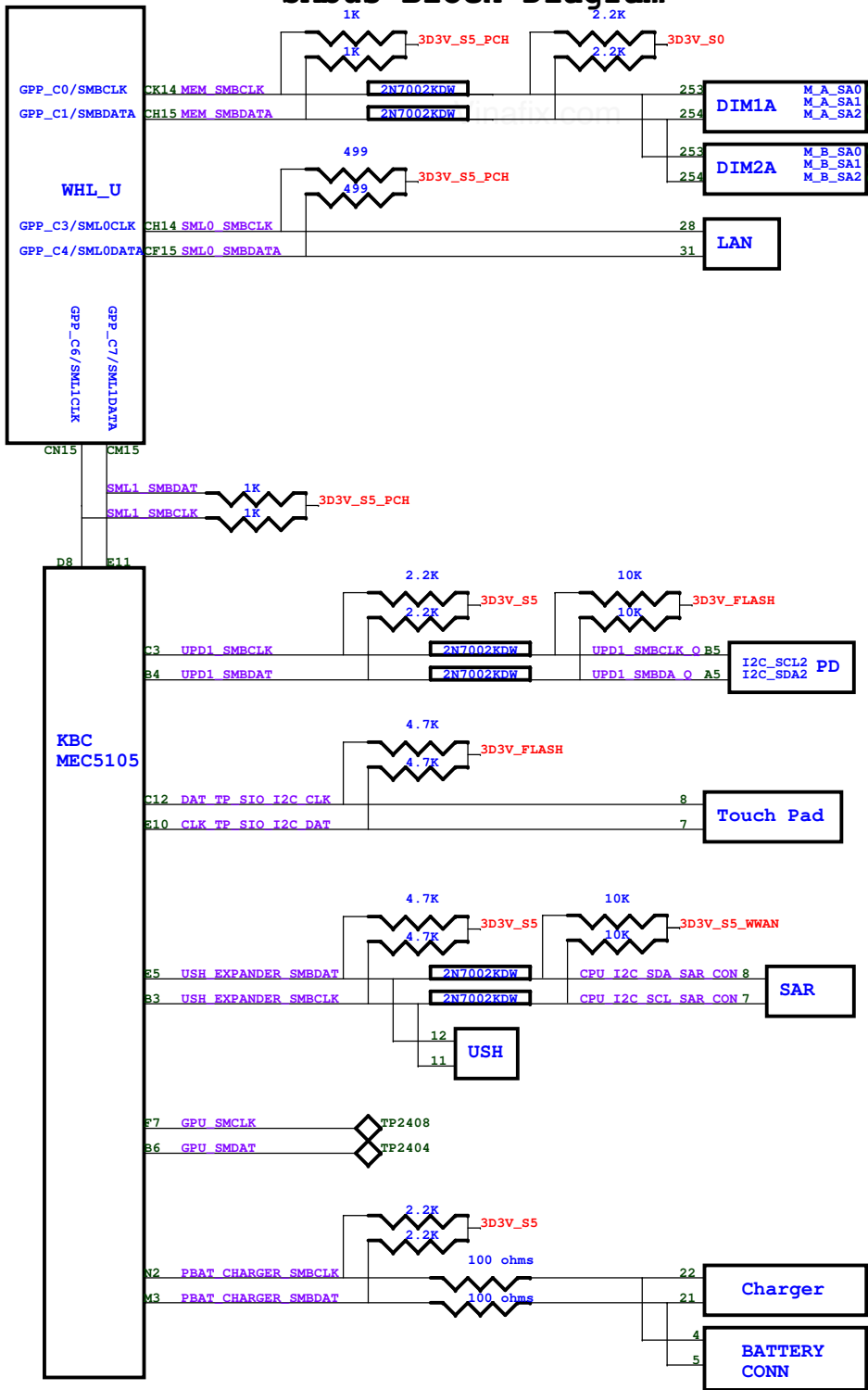


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SMBus Block Diagram



I2C Block Diagram

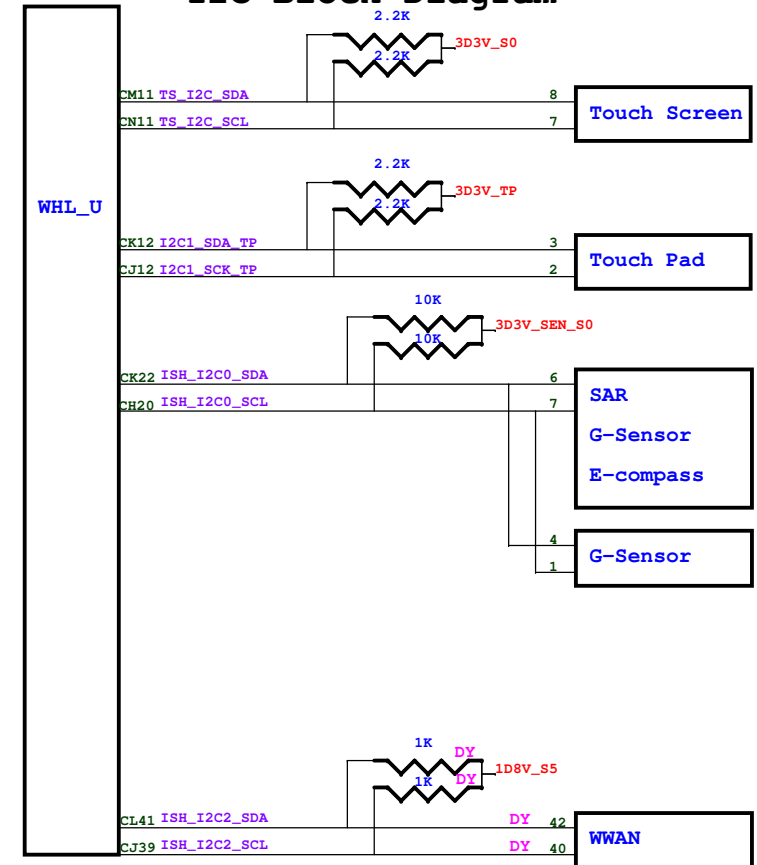


Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength

Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	28	O/d	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).
SMB_DATA	31	O/d	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).

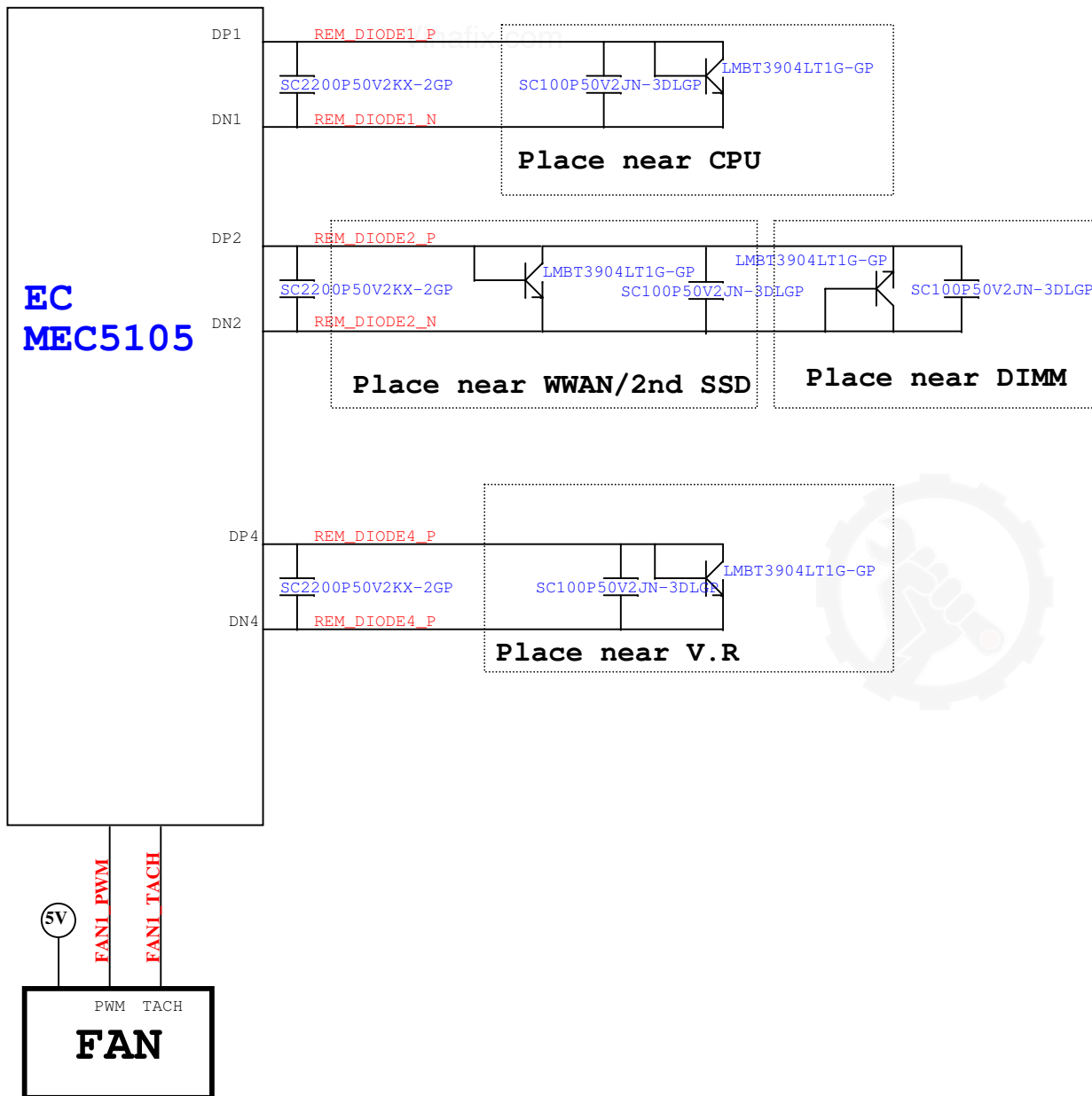
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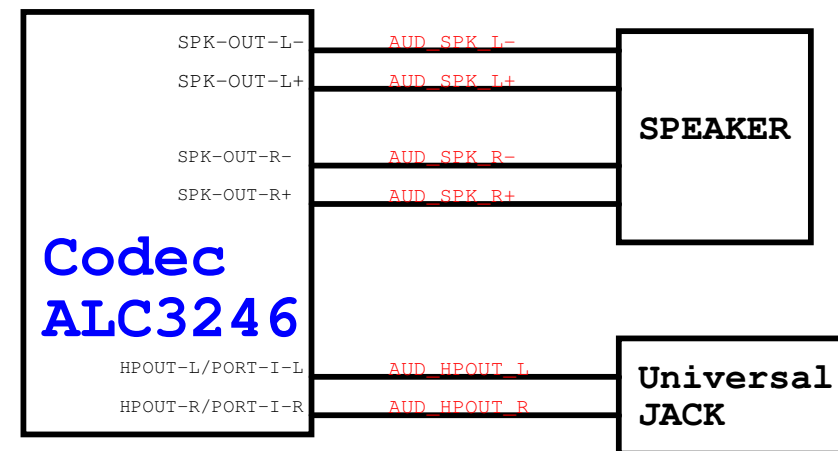
SMBUS/I2C BLOCK DIAGRAM

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Thermal Block Diagram



Audio Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**


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